**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**
**BOARD OF PATENT APPEALS AND INTERFERENCES**

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| In Re Application of:<br>**Arturo A. Rodriguez** | Confirmation No. **8279** |
| Serial No.:<br>**09/736,661** | Group Art Unit:<br>**2621** |
| Filed:<br>**December 14, 2000** | Examiner:<br>**An, Shawn S.** |
| For:<br>**System and Method for Adaptive Video Processing with Coordinated Resource Allocation** | Docket No.:<br>**60374.0052USU1/ CPOL 967732** |

## APPEAL BRIEF UNDER 37 C.F.R. § 41.37

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is an appeal from the final Office Action dated March 9, 2010 (Paper No./Mail Date 20100228), which rejected claims 38, 53-55, 71-78, 80-82, and 85-89 in the present application. Appellants filed a Notice of Appeal on June 17, 2010 with an appropriate petition for extension of time. The present Appeal Brief is a follow-up to the filed Notice of Appeal.

## I. REAL PARTY IN INTEREST

The real party in interest of the instant application is Scientific-Atlanta, LLC, having its principal place of business at 5030 Sugarloaf Parkway, Lawrenceville, GA 30044. Scientific-Atlanta, LLC, the assignee of record, is wholly owned by Cisco Technology, Inc.

## II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

## III. STATUS OF THE CLAIMS

Claims 38, 53-55, 71-78, 80-82, and 85-89 stand finally rejected by the final Office Action dated March 9, 2010, and are the subject of this appeal. Claims 1-37, 39-52, 56-70, 79, and 83-84 were cancelled during prosecution.

## IV. STATUS OF AMENDMENTS

No claim amendments have been submitted after the final Office Action, and all amendments made before the final Office Action have been entered. The claim listing in section VIII (CLAIMS – APPENDIX, below) represents the present state of the claims.

## V. SUMMARY OF THE CLAIMED SUBJECT MATTER

Embodiments of the claimed subject matter are summarized below with reference numbers and references to the written description ("specification") and drawings. The subject matter described below appears in the original disclosure at least where indicated, and may further appear in other places within the original disclosure.

Embodiments of the claimed subject matter, such as those defined by independent claim 38, define a method for adapting to resource constraints of a digital home communication terminal (DHCT) (see, e.g., FIG. 2, reference numeral 16; page 7, lines 14-26), said method comprising steps of: determining by the DHCT whether one of a resource-constrained mode or a non-resource constrained mode is to be initiated, the DHCT capable of operating in the non-resource constrained mode and a plurality of resource constrained modes (see, e.g., page 13, lines 1-6; page 15, lines 25-32; page 16, lines 13-14; page 17, line 7 – page 18, line 21; page 23, line 1 – page 31, line 19); responsive to determining that one of the resource-constrained modes is to be initiated, operating the DHCT in the determined resource-constrained mode (see, e.g., page 26, lines 5-9), including: retrieving a set of reconstructed decompressed video frames from a first portion (see, e.g., FIG. 5, reference numeral 30; page 26, lines 5-18) of a memory component (see, e.g., FIG. 5, reference numeral 60; page 13, line 31 – page 14, line 8), wherein the memory component stores compressed video frames in a distinct second portion (see, e.g., FIG. 5, reference numeral 62), wherein the set of video frames corresponds to a video picture stored in the first portion; and transferring the set of retrieved reconstructed decompressed video frames to a display device while downscaling the video picture in transit to the display device (see, e.g., page 26, line 5 – page 27, line 15).

Embodiments of the claimed subject matter, such as those defined by independent claim 53, define a method for adapting to resource constraints of a digital communication terminal (DHCT) (see, e.g., FIG. 2, reference numeral 16; page 7, lines 14-26), said method comprising steps of: determining by the DHCT whether one of a plurality of resource-constrained modes is to be initiated, the DHCT capable of operating in a non-resource constrained mode and the plurality of resource-constrained modes (see, e.g., page 13, lines 1-6; page 15, lines 25-32; page 16, lines 13-14; page 17, line 7 – page 18, line 21; page 23, line 1 – page 31, line 19); responsive to determining that one of the resource-constrained modes is to

be initiated, initiating the resource-constrained mode (see, e.g., page 26, lines 5-9), including: retrieving, from a first portion (see, e.g., FIG. 5, reference numeral 62; page 14, lines 1-8; page 16, lines 25-32) of a memory component (see, e.g., FIG. 5, reference numeral 60; page 13, line 31 – page 14, line 8), a set of compressed frames; storing, in a second and distinct portion (see, e.g., FIG. 5, reference numeral 30; page 14, lines 1-8) of the memory component, a set of decoded frames corresponding to the set of compressed frames, each of the set of decoded frames being at a first spatial resolution; retrieving, from the second and distinct portion of the memory component, the set of decoded frames (see, e.g., page 26, lines 5-32); and transferring the retrieved set of decoded frames to a display device while scaling the frames in transit to the display device to a second spatial resolution without storing the frames in the memory component, wherein the second spatial resolution is smaller than the first spatial resolution (see, e.g., page 26, lines 5 – page 27, line 15).

Embodiments of the claimed subject matter, such as those defined by independent claim 54, define a digital home communication terminal (DHCT) (see, e.g., FIG. 2, reference numeral 16; page 7, lines 14-26) comprising: a processor (see, e.g., FIG. 2, reference numeral 44; page 27, line 27); a circuit (see, e.g., FIG. 6, reference numeral 80; page 13, lines 1-6; page 25, line 28) configured to operate in a non-resource constrained mode and a plurality of resource-constrained modes, the circuit, responsive to instantiation of operation in the resource-constrained mode, configured in cooperation with the processor to: retrieve, from a first portion (see, e.g., FIG. 5, reference numeral 62; page 14, lines 1-8; page 16, lines 25-32) of a memory component (see, e.g., FIG. 5, reference numeral 60; page 13, line 31 – page 14, line 8), a set of compressed frames; store, in a second and distinct portion (see, e.g., FIG. 5, reference numeral 30; page 14, lines 1-8) of the memory component, a set of decoded frames corresponding to the set of compressed frames, each of the set of decoded frames being at a first spatial resolution; retrieve, from the memory component, the set of decoded frames (see, e.g., page 26, lines 5-

32); and transfer the set of decoded frames to a display device while scaling the frames in transit to the display device to a second spatial resolution without storing the frames in the memory component, wherein the second spatial resolution is smaller than the first spatial resolution (see, e.g., page 26, lines 5 – page 27, line 15).

Embodiments of the claimed subject matter, such as those defined by independent claim 55, define a method for adapting to resource constraints of a digital home communication terminal (DHCT) (see, e.g., FIG. 2, reference numeral 16; page 7, lines 14-26), said method comprising steps of: operating the DHCT in either a non-resource constrained mode or one of a plurality of resource-constrained modes, the DHCT capable of operating in the non-resource constrained mode and the plurality of resource-constrained modes (see, e.g., page 13, lines 1-6; page 25, line 28); receiving, in a memory component (see, e.g., FIG. 5, reference numeral 60; page 13, line 31 – page 14, line 8), video frames each comprising a complete picture; determining whether one of the resource-constrained modes is to be initiated (see, e.g., page 13, lines 1-6; page 15, lines 25-32; page 16, lines 13-14; page 17, line 7 – page 18, line 21; page 23, line 1 – page 31, line 19); responsive to determining that one of the resource-constrained modes is to be initiated, initiating the resource-constrained mode, including: retrieving the video frames from the memory component (see, e.g., page 26, lines 5-32); and transferring the retrieved video frames to a display device while downscaling the retrieved video frames in transit to the display device (see, e.g., page 26, lines 5 – page 27, line 15).

Embodiments of the claimed subject matter, such as those defined by independent claim 89, define a method comprising retrieving, from a first portion (see, e.g., FIG. 5, reference numeral 62; page 14, lines 1-8; page 16, lines 25-32) of a memory component (see, e.g., FIG. 5, reference numeral 60; page 13, line 31 – page 14, line 8), a set of compressed frames; storing, in a second and distinct portion (see, e.g., FIG. 5, reference numeral 30; page 14, lines 1-8) of the memory component, a set of decoded frames corresponding to the set of

compressed frames, each of the set of decoded frames being at a first spatial resolution; retrieving, from the second and distinct portion of the memory component, the set of decoded frames (see, e.g., page 26, lines 5-32); and transferring the retrieved set of decoded frames to a display device while scaling the frames in transit to the display device to a second spatial resolution without storing the frames in the memory component, wherein the second spatial resolution is smaller than the first spatial resolution (see, e.g., page 26, lines 5 – page 27, line 15).

## VI. GROUND OF REJECTION TO BE REVIEWED ON APPEAL

The following ground of rejection is to be reviewed on appeal.

A. Claims 38, 53-55, 71-78, 80-82, and 85-89 have been rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over U.S. Patent No. 6,570,579 to *MacInnis et al.* ("*MacInnis*") in view of U.S. Patent No. 5,614,952 to *Boyce et al.* ("*Boyce*") and U.S. Patent No. 5,953,506 to *Kalra et al.* ("*Kalra*").

## VII. ARGUMENT

### A. Claims 38, 53-55, 71-78, 80-82, and 85-89 - 35 U.S.C. § 103(a) - *MacInnis*, *Boyce*, *Kalra*.

The following rule of law is applicable to all 35 U.S.C. § 103(a). The U.S. Patent and Trademark Office ("USPTO") has the burden under section 103 to establish a *prima facie* case of obviousness according to the factual inquiries expressed in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966). The four factual inquires, also expressed in MPEP 2100-116, are as follows:

(A) Determining the scope and contents of the prior art;

(B) Ascertaining the differences between the prior art and the claims in issue;

(C) Resolving the level of ordinary skill in the pertinent art; and

(D) Evaluating evidence of secondary considerations.

Appellants respectfully submit that a *prima facie* case of obviousness is not established using the art of record.

1. Independent Claim 38 and dependent claims 71-73 and 85

Claim 38 recites (with emphasis added):

> 38. A method for adapting to resource constraints of a digital home communication terminal (DHCT), said method comprising steps of:
> determining by the DHCT whether one of a resource-constrained mode or a non-resource constrained mode is to be initiated, the DHCT capable of operating in the non-resource constrained mode and a plurality of resource constrained modes;
> responsive to determining that one of the resource-constrained modes is to be initiated, operating the DHCT in the determined resource-constrained mode, including:
> ***retrieving a set of reconstructed decompressed video frames from a first portion of a memory component, wherein the memory component stores compressed video frames in a distinct second portion, wherein the set of video frames corresponds to a video picture stored in the first portion***; and
> ***transferring the set of retrieved reconstructed decompressed video frames to a display device while downscaling the video picture in transit to the display device***.

Appellants respectfully submit that claim 38 is allowable over the combination of *MacInnis* in view of *Boyce* and *Kalra*. Briefly, claim 38 comprises elements that are arranged to cover at least one embodiment where a compressed picture buffer and decoded picture buffer reside in media memory, and downscaling is implemented on the video picture in transit between the decoded picture buffer and the display device. In contrast, Appellants respectfully submit that the cited art of record operates in a fundamentally different manner.

For instance, with regard to *MacInnis*, the final Office Action (page 4) acknowledges that *MacInnis* does not "seem to particularly disclose the memory component storing compressed

video data in a distinct second portion," and further acknowledges (page 3, emphasis in original) that *MacInnis* "does not seem to particularly disclose transferring the set of retrieved reconstructed decompressed video frames to a display device ***while*** *downscaling the video picture in transit to the display device*." Though *MacInnis* appears to focus attention on primarily graphics processing, *MacInnis* describes video decoding and capture and scaling at least in association with Figure 5 (reproduced below).



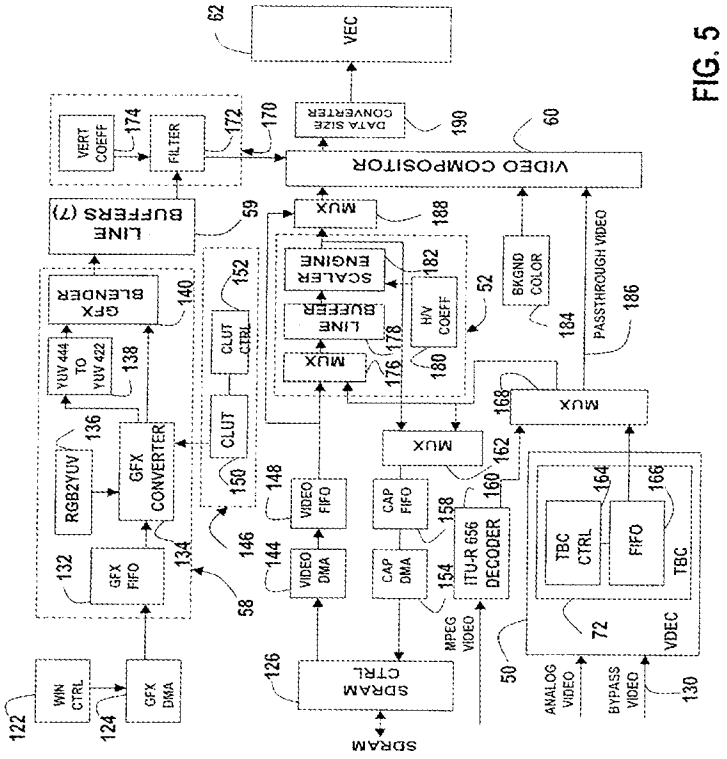



FIG. 5

In particular, col. 11, lines 39 – col. 12, line 7 of *MacInnis* provides as follows (emphasis added):

> Analog video or MPEG video may be provided to the video compositor as passthrough video. Alternatively, either type of video may be <u>captured into</u>

> memory and provided to the video compositor as a scaled video window. The digitized analog video signals preferably have a pixel sample rate of 13.5 MHz, contain a 16 bit data stream in YUV 4:2:2 format, and include timing signals such as top field and vertical sync signals.
>
> The VDEC 50 includes a time base corrector (TBC) 72 comprising a TBC controller 164 and a FIFO 166. To provide passthrough video that is synchronized to a display clock preferably without using a frame buffer, the digitized analog video is corrected in the time domain in the TBC 72 before being blended with other graphics and video sources. During time base correction, the video input which runs nominally at 13.5 MHZ is synchronized with the display clock which runs nominally at 13.5 MHZ at the output; these two frequencies that are both nominally 13.5 MHz are not necessarily exactly the same frequency. In the TBC, the video output is preferably offset from the video input by a half scan line per field.
>
> A capture FIFO 158 and a capture DMA 154 preferably capture the digitized analog video signals and MPEG video. The SDRAM controller 126 provides captured video frames to the external SDRAM. A video DMA 144 transfers the captured video frames to a video FIFO 148 from the external SDRAM.
>
> The digitized analog video signals and MPEG video are preferably scaled down to less than 100% prior to being captured and are scaled up to more than 100% after being captured. The video scaler 52 is shared by both upscale and downscale operations. The video scaler preferably includes a multiplexer 176, a set of line buffers 178, a horizontal and vertical coefficient memory 180 and a scaler engine 182. The scaler engine 182 preferably includes a set of two polyphase filters, one for each of horizontal and vertical dimensions.

In other words, it is clear that any alleged "downscaling" occurs prior to capture, not post-capture as described in association with claim 38. Such operation is consistent with *MacInnis*' expressed benefit (see Summary) of conserving memory.

The final Office Action (page 2, "Response to Remarks," emphasis in original) provides as follows:

> Moreover, please note Macinnis et al discloses video decoder (Fig. 2, 50) to the video scaler (Fig. 2, 52), wherein the scaler may perform both downscaling and upscaling of digital/analog video as needed (col. 5, lines 65-66), which is substantially the same/similar as Applicant's decoder (Fig. 4, 81) to the video scaler (83). Therefore, Macinnis et al discloses downscaling after decompressed video frames/pictures.

Appellants respectfully disagree. FIG. 2 of *MacInnis* provides as follows:

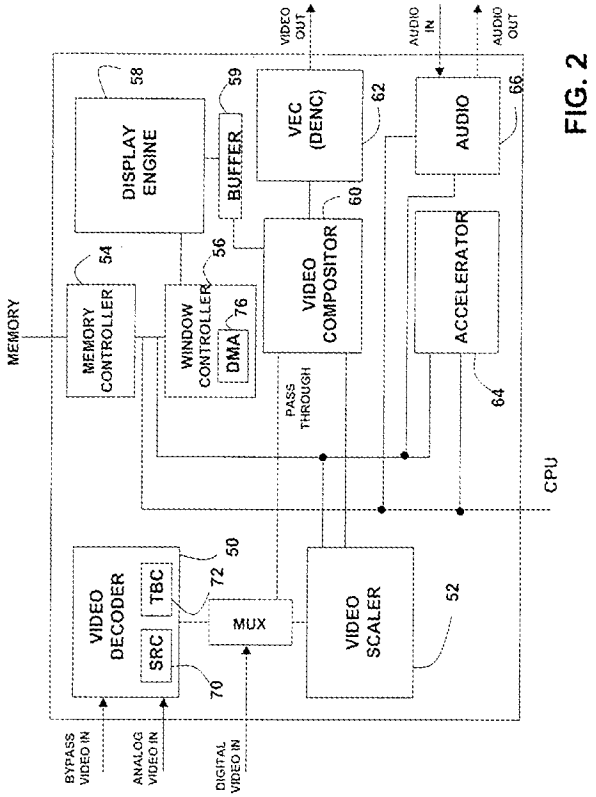



FIG. 2

Reviewing the architecture shown in Figure 2 of *MacInnis*, it is noted that analog and digital video enters at the decoder 50 and the mux, respectively. Further, column 5, 65-66 of *MacInnis* provides as follows:

> The video scaler 52 may perform both downscaling and upscaling of digital video and analog video as needed.

In other words, from this provision and Figure 2 of *MacInnis*, it appears that scaling is performed on the analog or video inputs. More telling of the functionality performed by the architecture in Figure 2 is the description set forth in the same paragraph in column 6, lines 4-9 of *MacInnins*, reproduced below (emphasis added):

> Any portion of the input may be the source for video scaling. To conserve memory and bandwidth, the video scaler preferably downscales before capturing video frames to memory, and upscales after reading from memory, but preferably does not perform both upscaling and downscaling at the same time.

In other words, scaling operations in *MacInnis* appear to be intended, at least in part, to reduce memory consumption. Further, these excerpts also highlight the differences to the claims of the present application, the latter being in the context of scaling operations performed on video already saved to memory. The reference in the above-reproduced section of the final Office Action to the alleged similarity to Appellants' decoder in Figure 4 ignores the fact that the decoder in Figure 4 of Appellants' disclosure acts on video stored in media memory 60 and is passed to the media engine 80 that encompasses the video decoder via the media memory bus, and further, that the scaling operation in Appellant's claimed embodiment is implemented downstream of the media memory, unlike that shown in Figure 2 of *MacInnis*.

Likewise, *Kalra*, though apparently used for alleged teaching of the various mode operations as described in claim 38, appears to scale the video in the network (by sending base and additive streams based on a profile provided by the client (see Summary, e.g., col. 2, lines 27-49, *Kalra*), addressing the presence of clients of differing capabilities in a network (see Background, e.g., col. 1, lines 21-58, *Kalra*). In other words, any reduction of resolution via scaling occurs pre-capture, not post-capture as claimed.

With regard to *Boyce*, the final Office Action (page 4) alleges the following (emphasis in original):

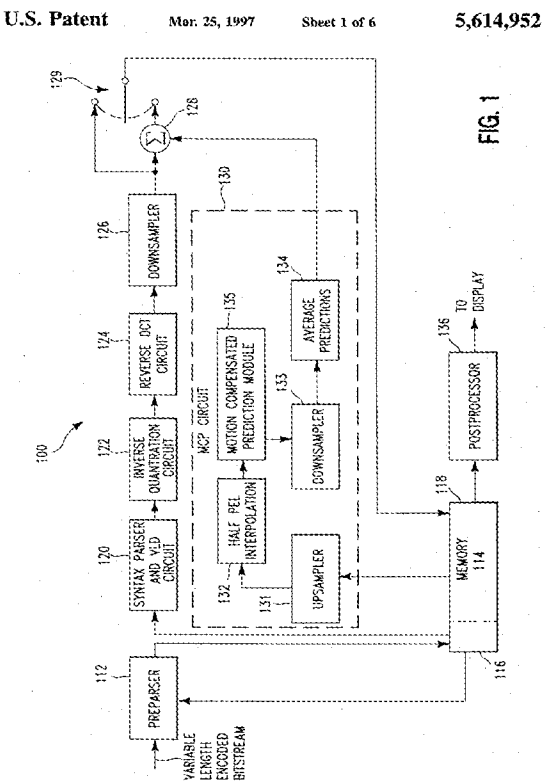
> Furthermore, Boyce et al teaches digital video decoder comprising retrieving a set of reconstructed decompressed (decoded) video data from a first portion (Fig. 1, 118) of a memory component (114), wherein the memory component stores compressed video data in a distinct second portion (116), wherein the set of video data corresponds to a video picture (col. 4, lines 64-67; col. 5, lines 1-4; col. 10, lines 44-50) for efficiently managing the memory resources such as size or the bandwidth (col. 10, lines 1-4).
>
> Moreover, Boyce et al teaches transferring the set of retrieved reconstructed decompressed (decoded) video data (from Fig. 4, 402 and 403) to a display device (TO DISPLAY) ***while*** downscaling (Reduced Resolution) the video picture

> in transit to the display device for implementing picture-in-picture capabilities in a digital TV without incurring the cost of multiple full resolution decoders (Fig. 4, col. 17, lines 66-67; col. 18, lines 12-38; col. 2, lines 37-40).

Appellants respectfully submit that *Boyce*, like *MacInnis* and *Kalra*, fails to describe downscaling after the decompressed picture buffer. It is noteworthy that the reduced resolution decoders 402 and 403 of FIG. 4 are used in the final Office Action to support the alleged teachings of downscaling in transit. However, Appellants believe that *Boyce* teaches that the decoders 402 and 403 are based on the operations and architecture of the decoder circuit 100 shown, for instance in Figure 1 of *Boyce*. For instance, *Boyce* describes the decoders 402 and 403 as containing components of the decoder circuit 100 (reproduced below), such as the IDCT circuit 124 (col. 18, line 16, *Boyce*), the IQ circuit 122 (col. 18, line 28, *Boyce*), and preparser 112 (col. 18, lines 39-46, *Boyce*). Further, the decoders 402 and 403 are described in col. 18, lines 33-38 of *Boyce* as follows (emphasis added):

> In accordance with the present invention, the reduced resolution decoders 402, 403 store the low resolution frames in their reduced size. Thus, by using 2.times.2 DCT coefficient blocks the size of the frame buffers can be about 1/16th of the size that would be required if 8.times.8 DCT coefficient blocks, i.e., full resolution blocks, were stored.

In other words, the decoders 402 and 403 not only store frames in reduced resolution format (and hence do NOT teach downscaling after the decompressed picture buffer), but also appear to share the same architecture as the decoder circuit 100. Figure 1 of *Boyce* is reproduced below:




The following excerpts from *Boyce* (reproduced below) support Appellants' position that *Boyce* (like *Kalra* and *MacInnis*) operates in a fundamentally different manner than claimed (emphasis added):

> *Col. 4, lines 34-39*: The method of the present invention for decoding HD and SD pictures includes the steps of reducing the resolution of received HD pictures prior to decoding by using, e.g., a preparser unit and/or adaptive field/frame downsampling to reduce the complexity of later processing stages of the decoder.
>
> *Col. 5, lines 25-44*: Because the cost and complexity of a HDTV decoder is largely a function of the requirement that it process large amounts of data on a real time basis, it is possible to reduce the complexity and thus the cost of a HDTV compatible decoder by reducing the amount of data that needs to be processed. While using only a small portion of the video data received in an HDTV signal will result in reduced resolution and picture quality, by carefully selecting which HDTV data to process and the method by which it is processed, video image quality comparable to or better than SD television signals can be achieved. As will be discussed below, the preparser 112 serves to dynamically limit the amount of video data supplied to the remaining elements of the decoder

> circuit 100 including the syntax parser and VLD circuit 120 thereby reducing the amount of data that must be processed by the subsequent circuit elements on a real time basis and the required complexity of those circuit elements. An additional benefit of the use of the preparser 112 is that it permits for the use of a smaller coded data buffer 116 than would otherwise be required.
>
> *Col. 9, line 61 – col. 10, line 5*: The output of the IDCT circuit 124 is coupled to the input of the downsampler 126. The downsampler 126 is used to downsample the data corresponding to each picture prior to storage in the frame buffer 118. As a result of the downsampling operation, the amount of data required to represent a video frame is substantially reduced. For example if the downsampler 126 is implemented to remove half of the digital samples used to represent a picture, the amount of data that would have to be stored will be reduced by a factor of approximately two substantially reducing the amount of memory required to implement the frame buffer 118.
>
> *Col. 11, lines 39-46*: In accordance with the present invention, the downsampled frames supplied by the frame buffer 118 to the MCP circuit 130 are upsampled, e.g., on-the-fly, interpolated and then downsampled prior to generating predictions based on the motion vectors. In this manner the motion vectors which were originally generated based on full resolution video frames are effectively applied to downsampled video frames.

These excerpts from *Boyce* reveal that downsampling does not occur post-capture in a decoded picture buffer, but rather, pre-capture. The final Office Action (page 2, "Response to Remarks") provides as follows:

> Moreover, Boyce et al not only teaches storing frames in reduce resolution, but also teaches downscaling by performing IDCT (inverse discrete cosine transform) and IQ (inverse quantization)(col. 18, lines 12-38). In other words, the reduced resolution decoder inherently has to downscale a standard frame into a much smaller size frame in order to display the reduced frame into the main frame itself as a picture in picture format as discussed above.

Col. 18, lines 12-38 of *Boyce* provides as follows:

> In one embodiment of the present invention the size of the reduced resolution pictures incorporated into the main picture is selected to be 1/4.times.1/4 the size of the normal picture. In such an embodiment, each MPEG 8.times.8 pixel block need only be decoded to a size corresponding to a block of 2.times.2 pixels.
>
> The cost of the IDCT circuit 124 used in the reduced resolution decoders 402, 403 can be substantially reduced in accordance with the present invention by performing the IDCT operations on only 2.times.2 blocks as opposed to 8.times.8 blocks. This is achieved by, e.g., retaining and processing only the upper left 2.times.2 block of DCT coefficients of each 8.times.8 DCT coefficient block of a HDTV picture with all the other DCT coefficients being set to zero. Accordingly, in

> such an embodiment, the IDCT circuit cost is reduced to approximately the cost of a circuit which can perform a 2.times.2 IDCT as opposed to an 8.times.8 IDCT.
>
> The IQ circuit 122 of the reduced resolution decoders 402, 403 can be simplified in a similar manner with the IQ circuit 122 operating only on a 2.times.2 block of DCT coefficients, i.e., 4 coefficient values, as opposed to 64 DCT coefficient values that form an 8.times.8 DCT coefficient block.
>
> In accordance with the present invention, the reduced resolution decoders 402, 403 store the low resolution frames in their reduced size. Thus, by using 2.times.2 DCT coefficient blocks the size of the frame buffers can be about 1/16th of the size that would be required if 8.times.8 DCT coefficient blocks, i.e., full resolution blocks, were stored.

Nothing in the section recited above suggests downscaling post capture. Indeed, the reference to IDCT and IQ components is misplaced, since those components are shown in Figure 1 of *Boyce* as receiving compressed pictures (section 116 is a "coded data buffer" that is "used for the temporary storage of the compressed bitstream" – see, col. 4, line 67 – col. 5, line 1, *Boyce*), and hence cannot constitute the retrieval of reconstructed frames as claimed. For at least these reasons, Appellants respectfully submit that claim 38 is allowable over *MacInnis* in view of *Boyce* and *Kalra* and respectfully request that the rejection be overturned.

Because independent claim 38 is allowable over *MacInnis* in view of *Boyce* and *Kalra*, dependent claims 71-73 and 85 are allowable as a matter of law for at least the reason that the dependent claims 71-73 and 85 contain all elements of their respective base claim. See, *e.g.*, *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988). Accordingly, Appellants respectfully request that the rejection to dependent claims 71-73 and 85 be overturned for similar reasons expressed above for claim 38.

2. Independent claim 53 and dependent claims 74-77 and 86

Claim 53 recites (with emphasis added):

> 53. A method for adapting to resource constraints of a digital communication terminal (DHCT), said method comprising steps of:

> determining by the DHCT whether one of a plurality of resource-constrained modes is to be initiated, the DHCT capable of operating in a non-resource constrained mode and the plurality of resource-constrained modes;
>
> responsive to determining that one of the resource-constrained modes is to be initiated, initiating the resource-constrained mode, including:
>
> retrieving, from a first portion of a memory component, a set of compressed frames;
>
> storing, in a second and distinct portion of the memory component, a set of decoded frames corresponding to the set of compressed frames, each of the set of decoded frames being at a first spatial resolution;
>
> ***retrieving, from the second and distinct portion of the memory component, the set of decoded frames; and***
>
> ***transferring the retrieved set of decoded frames to a display device while scaling the frames in transit to the display device to a second spatial resolution without storing the frames in the memory component, wherein the second spatial resolution is smaller than the first spatial resolution***.

Appellants respectfully submit that claim 53 is allowable over the combination of *MacInnis* in view of *Boyce* and *Kalra*. Briefly, claim 53 comprises elements that are arranged to cover at least one embodiment where a compressed picture buffer and decoded picture buffer reside in media memory, and downscaling is implemented on the video picture in transit between the decoded picture buffer and the display device. In contrast, Appellants respectfully submit that the cited art of record operates in a fundamentally different manner.

For instance, with regard to *MacInnis*, the final Office Action (page 6) acknowledges that *MacInnis* does not "seem to particularly disclose the memory component storing and retrieving a set of decoded pictures in a distinct second portion," and further acknowledges (page 6, emphasis in original) that *MacInnis* "does not seem to particularly disclose…transferring a set of retrieved decoded pictures to a display device ***while*** *scaling the video picture in transit to the display device to a second spatial resolution* ***without*** *storing pictures in a memory component,* wherein the second spatial resolution is smaller than the first spatial resolution." Though *MacInnis* appears to focus attention on primarily graphics processing, *MacInnis* describes video decoding and capture and scaling at least in association with Figure 5 (reproduced below).

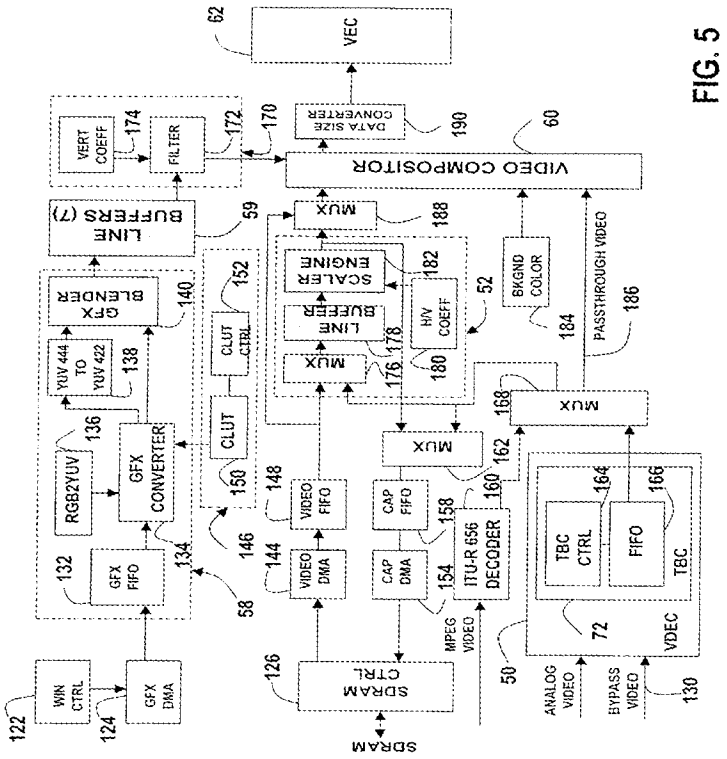



FIG. 5

In particular, col. 11, lines 39 – col. 12, line 7 of *MacInnis* provides as follows (emphasis added):

> Analog video or MPEG video may be provided to the video compositor as passthrough video. Alternatively, either type of video may be captured into memory and provided to the video compositor as a scaled video window. The digitized analog video signals preferably have a pixel sample rate of 13.5 MHz, contain a 16 bit data stream in YUV 4:2:2 format, and include timing signals such as top field and vertical sync signals.
>
> The VDEC 50 includes a time base corrector (TBC) 72 comprising a TBC controller 164 and a FIFO 166. To provide passthrough video that is synchronized to a display clock preferably without using a frame buffer, the digitized analog video is corrected in the time domain in the TBC 72 before being blended with other graphics and video sources. During time base correction, the video input which runs nominally at 13.5 MHZ is synchronized with the display clock which runs nominally at 13.5 MHZ at the output; these two frequencies that

> are both nominally 13.5 MHz are not necessarily exactly the same frequency. In the TBC, the video output is preferably offset from the video input by a half scan line per field.
>
> A capture FIFO 158 and a capture DMA 154 preferably capture the digitized analog video signals and MPEG video. The SDRAM controller 126 provides captured video frames to the external SDRAM. A video DMA 144 transfers the captured video frames to a video FIFO 148 from the external SDRAM.
>
> The digitized analog video signals and MPEG video are preferably scaled down to less than 100% prior to being captured and are scaled up to more than 100% after being captured. The video scaler 52 is shared by both upscale and downscale operations. The video scaler preferably includes a multiplexer 176, a set of line buffers 178, a horizontal and vertical coefficient memory 180 and a scaler engine 182. The scaler engine 182 preferably includes a set of two polyphase filters, one for each of horizontal and vertical dimensions.

In other words, it is clear that any alleged "downscaling" (i.e., in claim 53, scaling that results in a smaller resolution than the first resolution from which it derives) occurs prior to capture, not post-capture as described in association with claim 53. Such operation is consistent with *MacInnis*' expressed benefit (see Summary) of conserving memory.

The final Office Action (page 2, "Response to Remarks," emphasis in original) provides as follows:

> Moreover, please note Macinnis et al discloses video decoder (Fig. 2, 50) to the video scaler (Fig. 2, 52), wherein the scaler may perform both downscaling and upscaling of digital/analog video as needed (col. 5, lines 65-66), which is substantially the same/similar as Applicant's decoder (Fig. 4, 81) to the video scaler (83). Therefore, Macinnis et al discloses downscaling after decompressed video frames/pictures.

Appellants respectfully disagree. FIG. 2 of *MacInnis* provides as follows:

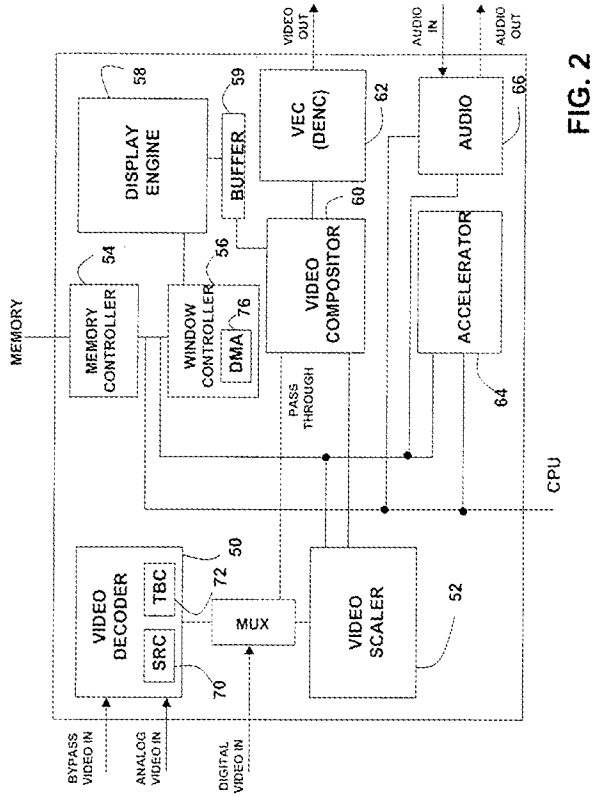



FIG. 2

Reviewing the architecture shown in Figure 2 of *MacInnis*, it is noted that analog and digital video enters at the decoder 50 and the mux, respectively. Further, column 5, 65-66 of *MacInnis* provides as follows:

> The video scaler 52 may perform both downscaling and upscaling of digital video and analog video as needed.

In other words, from this provision and Figure 2 of *MacInnis*, it appears that scaling is performed on the analog or video inputs. More telling of the functionality performed by the architecture in Figure 2 is the description set forth in the same paragraph in column 6, lines 4-9 of *MacInnins*, reproduced below (emphasis added):

> Any portion of the input may be the source for video scaling. To conserve memory and bandwidth, the video scaler preferably downscales before capturing video frames to memory, and upscales after reading from memory, but preferably does not perform both upscaling and downscaling at the same time.

In other words, scaling operations in *MacInnis* appear to be intended, at least in part, to reduce memory consumption. Further, these excerpts also highlight the differences to the claims of the present application, the latter being in the context of scaling operations performed on video already saved to memory. The reference in the above-reproduced section of the final Office Action to the alleged similarity to Appellants' decoder in Figure 4 ignores the fact that the decoder in Figure 4 of Appellants' disclosure acts on video stored in media memory 60 and is passed to the media engine 80 that encompasses the video decoder via the media memory bus, and further, that the scaling operation in Appellant's claimed embodiment is implemented downstream of the media memory, unlike that shown in Figure 2 of *MacInnis*.

Likewise, *Kalra*, though apparently used for alleged teaching of the various mode operations as described in claim 53, appears to scale the video in the network (by sending base and additive streams based on a profile provided by the client (see Summary, e.g., col. 2, lines 27-49, *Kalra*), addressing the presence of clients of differing capabilities in a network (see Background, e.g., col. 1, lines 21-58, *Kalra*). In other words, any reduction of resolution via scaling occurs pre-capture, not post-capture as claimed.

With regard to *Boyce*, the final Office Action (page 6) alleges the following (emphasis in original):

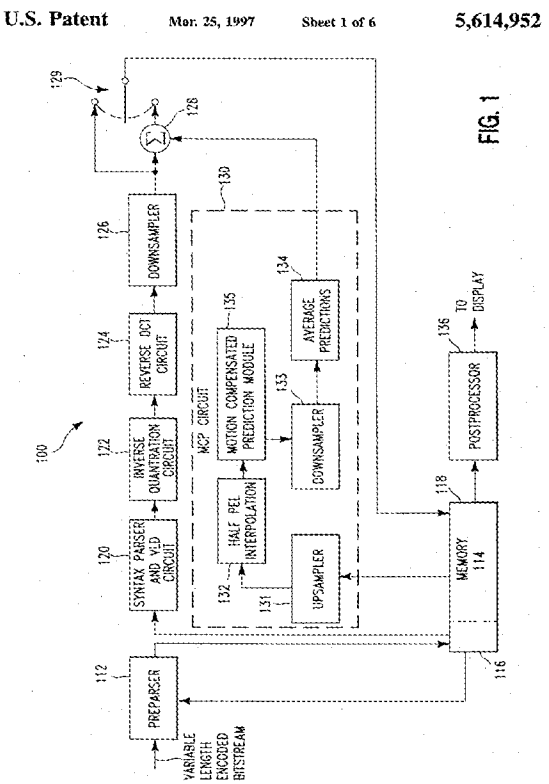
> Furthermore, Boyce et al teaches digital video decoder comprising retrieving a set of compressed pictures/frames from a first portion (Fig. 1, 116) of a memory component (114), wherein the memory component stores decoded video pictures/frames in a distinct second portion (116) of the memory component, wherein the set of video frames corresponding to video pictures/frames (col. 4, lines 64-67; col. 5, lines 1-4; col. 10, lines 44-50), and transferring a set of retrieved decoded pictures/frames (Fig. 4, 402, 403) to a display device (To Display) ***while*** scaling video pictures/frames in transit to the display device to a second spatial (reduced) resolution ***without*** storing pictures in a memory component, wherein the second spatial resolution is smaller than the first spatial resolution (from 401 or 402) for efficiently managing the memory resources such

> as size or the bandwidth (col. 10, lines 1-4) and implementing picture-in-picture capabilities in a digital TV without incurring the cost of multiple full resolution decoders (col. 17, lines 66-67; col. 18, lines 12-38; col. 2, lines 37-40).

Appellants respectfully submit that *Boyce*, like *MacInnis* and *Kalra*, fails to describe downscaling (e.g., scaling to a reduced resolution as claimed) after the decompressed picture buffer. It is noteworthy that the reduced resolution decoders 402 and 403 of FIG. 4 are used in the final Office Action to support the alleged teachings of downscaling in transit. However, Appellants believe that *Boyce* teaches that the decoders 402 and 403 are based on the operations and architecture of the decoder circuit 100 shown, for instance in Figure 1 of *Boyce*. For instance, *Boyce* describes the decoders 402 and 403 as containing components of the decoder circuit 100 (reproduced below), such as the IDCT circuit 124 (col. 18, line 16, *Boyce*), the IQ circuit 122 (col. 18, line 28, *Boyce*), and preparser 112 (col. 18, lines 39-46, *Boyce*). Further, the decoders 402 and 403 are described in col. 18, lines 33-38 of *Boyce* as follows (emphasis added):

> In accordance with the present invention, the reduced resolution decoders 402, 403 store the low resolution frames in their reduced size. Thus, by using 2.times.2 DCT coefficient blocks the size of the frame buffers can be about 1/16th of the size that would be required if 8.times.8 DCT coefficient blocks, i.e., full resolution blocks, were stored.

In other words, the decoders 402 and 403 not only store frames in reduced resolution format (and hence do NOT teach downscaling after the decompressed picture buffer), but also appear to share the same architecture as the decoder circuit 100. Figure 1 of *Boyce* is reproduced below:




The following excerpts from *Boyce* (reproduced below) support Appellants' position that *Boyce* (like *Kalra* and *MacInnis*) operates in a fundamentally different manner than claimed (emphasis added):

> *Col. 4, lines 34-39*: The method of the present invention for decoding HD and SD pictures includes the steps of reducing the resolution of received HD pictures prior to decoding by using, e.g., a preparser unit and/or adaptive field/frame downsampling to reduce the complexity of later processing stages of the decoder.
>
> *Col. 5, lines 25-44*: Because the cost and complexity of a HDTV decoder is largely a function of the requirement that it process large amounts of data on a real time basis, it is possible to reduce the complexity and thus the cost of a HDTV compatible decoder by reducing the amount of data that needs to be processed. While using only a small portion of the video data received in an HDTV signal will result in reduced resolution and picture quality, by carefully selecting which HDTV data to process and the method by which it is processed, video image quality comparable to or better than SD television signals can be achieved. As will be discussed below, the preparser 112 serves to dynamically limit the amount of video data supplied to the remaining elements of the decoder

> circuit 100 including the syntax parser and VLD circuit 120 thereby reducing the amount of data that must be processed by the subsequent circuit elements on a real time basis and the required complexity of those circuit elements. An additional benefit of the use of the preparser 112 is that it permits for the use of a smaller coded data buffer 116 than would otherwise be required.
>
> *Col. 9, line 61 – col. 10, line 5*: The output of the IDCT circuit 124 is coupled to the input of the downsampler 126. The downsampler 126 is used to downsample the data corresponding to each picture prior to storage in the frame buffer 118. As a result of the downsampling operation, the amount of data required to represent a video frame is substantially reduced. For example if the downsampler 126 is implemented to remove half of the digital samples used to represent a picture, the amount of data that would have to be stored will be reduced by a factor of approximately two substantially reducing the amount of memory required to implement the frame buffer 118.
>
> *Col. 11, lines 39-46*: In accordance with the present invention, the downsampled frames supplied by the frame buffer 118 to the MCP circuit 130 are upsampled, e.g., on-the-fly, interpolated and then downsampled prior to generating predictions based on the motion vectors. In this manner the motion vectors which were originally generated based on full resolution video frames are effectively applied to downsampled video frames.

These excerpts from *Boyce* reveal that downsampling does not occur post-capture in a decoded picture buffer, but rather, pre-capture. The final Office Action (page 2, "Response to Remarks") provides as follows:

> Moreover, Boyce et al not only teaches storing frames in reduce resolution, but also teaches downscaling by performing IDCT (inverse discrete cosine transform) and IQ (inverse quantization)(col. 18, lines 12-38). In other words, the reduced resolution decoder inherently has to downscale a standard frame into a much smaller size frame in order to display the reduced frame into the main frame itself as a picture in picture format as discussed above.

Col. 18, lines 12-38 of *Boyce* provides as follows:

> In one embodiment of the present invention the size of the reduced resolution pictures incorporated into the main picture is selected to be 1/4.times.1/4 the size of the normal picture. In such an embodiment, each MPEG 8.times.8 pixel block need only be decoded to a size corresponding to a block of 2.times.2 pixels.
>
> The cost of the IDCT circuit 124 used in the reduced resolution decoders 402, 403 can be substantially reduced in accordance with the present invention by performing the IDCT operations on only 2.times.2 blocks as opposed to 8.times.8 blocks. This is achieved by, e.g., retaining and processing only the upper left 2.times.2 block of DCT coefficients of each 8.times.8 DCT coefficient block of a HDTV picture with all the other DCT coefficients being set to zero. Accordingly, in

> such an embodiment, the IDCT circuit cost is reduced to approximately the cost of a circuit which can perform a 2.times.2 IDCT as opposed to an 8.times.8 IDCT.
>
> The IQ circuit 122 of the reduced resolution decoders 402, 403 can be simplified in a similar manner with the IQ circuit 122 operating only on a 2.times.2 block of DCT coefficients, i.e., 4 coefficient values, as opposed to 64 DCT coefficient values that form an 8.times.8 DCT coefficient block.
>
> In accordance with the present invention, the reduced resolution decoders 402, 403 store the low resolution frames in their reduced size. Thus, by using 2.times.2 DCT coefficient blocks the size of the frame buffers can be about 1/16th of the size that would be required if 8.times.8 DCT coefficient blocks, i.e., full resolution blocks, were stored.

Nothing in the section recited above suggests downscaling post capture. Indeed, the reference to IDCT and IQ components is misplaced, since those components are shown in Figure 1 of *Boyce* as receiving compressed pictures (section 116 is a "coded data buffer" that is "used for the temporary storage of the compressed bitstream" – see, col. 4, line 67 – col. 5, line 1, *Boyce*), and hence cannot constitute the retrieval of reconstructed frames as claimed. For at least these reasons, Appellants respectfully submit that claim 53 is allowable over *MacInnis* in view of *Boyce* and *Kalra* and respectfully request that the rejection be overturned.

Because independent claim 53 is allowable over *MacInnis* in view of *Boyce* and *Kalra*, dependent claims 74-77 and 86 are allowable as a matter of law. Accordingly, Appellants respectfully request that the rejection to dependent claims 74-77 and 86 be overturned for similar reasons expressed above for claim 53.

3. Independent claim 54 and dependent claims 78, 80-81, and 87

Claim 54 recites (with emphasis added):

> 54. A digital home communication terminal (DHCT) comprising:
> a processor;
> a circuit configured to operate in a non-resource constrained mode and a plurality of resource-constrained modes, the circuit, responsive to instantiation of operation in the resource-constrained mode, configured in cooperation with the processor to:

> retrieve, from a first portion of a memory component, a set of compressed frames;
>
> store, in a second and distinct portion of the memory component, a set of decoded frames corresponding to the set of compressed frames, each of the set of decoded frames being at a first spatial resolution;
>
> ***retrieve, from the memory component, the set of decoded frames; and***
>
> ***transfer the set of decoded frames to a display device while scaling the frames in transit to the display device to a second spatial resolution without storing the frames in the memory component, wherein the second spatial resolution is smaller than the first spatial resolution***.

Appellants respectfully submit that claim 54 is allowable over the combination of *MacInnis* in view of *Boyce* and *Kalra*. Briefly, claim 54 comprises elements that are arranged to cover at least one embodiment where a compressed picture buffer and decoded picture buffer reside in media memory, and downscaling is implemented on the video picture in transit between the decoded picture buffer and the display device. In contrast, Appellants respectfully submit that the cited art of record operates in a fundamentally different manner.

For instance, with regard to *MacInnis*, the final Office Action (page 6) acknowledges that *MacInnis* does not "seem to particularly disclose the memory component storing and retrieving a set of decoded pictures in a distinct second portion," and further acknowledges (page 6, emphasis in original) that *MacInnis* "does not seem to particularly disclose…transferring a set of retrieved decoded pictures to a display device ***while*** *scaling the video picture in transit to the display device to a second spatial resolution* ***without*** *storing pictures in a memory component,* wherein the second spatial resolution is smaller than the first spatial resolution." Though *MacInnis* appears to focus attention on primarily graphics processing, *MacInnis* describes video decoding and capture and scaling at least in association with Figure 5 (reproduced below).

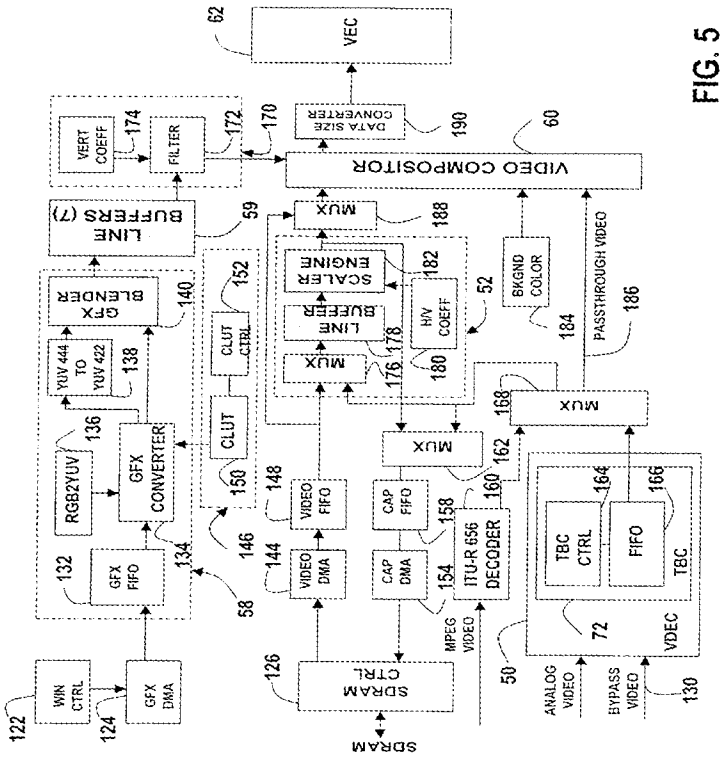



FIG. 5

In particular, col. 11, lines 39 – col. 12, line 7 of *MacInnis* provides as follows (emphasis added):

> Analog video or MPEG video may be provided to the video compositor as passthrough video. Alternatively, either type of video may be captured into memory and provided to the video compositor as a scaled video window. The digitized analog video signals preferably have a pixel sample rate of 13.5 MHz, contain a 16 bit data stream in YUV 4:2:2 format, and include timing signals such as top field and vertical sync signals.
>
> The VDEC 50 includes a time base corrector (TBC) 72 comprising a TBC controller 164 and a FIFO 166. To provide passthrough video that is synchronized to a display clock preferably without using a frame buffer, the digitized analog video is corrected in the time domain in the TBC 72 before being blended with other graphics and video sources. During time base correction, the video input which runs nominally at 13.5 MHZ is synchronized with the display clock which runs nominally at 13.5 MHZ at the output; these two frequencies that

> are both nominally 13.5 MHz are not necessarily exactly the same frequency. In the TBC, the video output is preferably offset from the video input by a half scan line per field.
>
> A capture FIFO 158 and a capture DMA 154 preferably capture the digitized analog video signals and MPEG video. The SDRAM controller 126 provides captured video frames to the external SDRAM. A video DMA 144 transfers the captured video frames to a video FIFO 148 from the external SDRAM.
>
> The digitized analog video signals and MPEG video are preferably scaled down to less than 100% prior to being captured and are scaled up to more than 100% after being captured. The video scaler 52 is shared by both upscale and downscale operations. The video scaler preferably includes a multiplexer 176, a set of line buffers 178, a horizontal and vertical coefficient memory 180 and a scaler engine 182. The scaler engine 182 preferably includes a set of two polyphase filters, one for each of horizontal and vertical dimensions.

In other words, it is clear that any alleged "downscaling" (i.e., in claim 54, scaling that results in a smaller resolution than the first resolution from which it derives) occurs prior to capture, not post-capture as described in association with claim 54. Such operation is consistent with *MacInnis*' expressed benefit (see Summary) of conserving memory.

The final Office Action (page 2, "Response to Remarks," emphasis in original) provides as follows:

> Moreover, please note Macinnis et al discloses video decoder (Fig. 2, 50) to the video scaler (Fig. 2, 52), wherein the scaler may perform both downscaling and upscaling of digital/analog video as needed (col. 5, lines 65-66), which is substantially the same/similar as Applicant's decoder (Fig. 4, 81) to the video scaler (83). Therefore, Macinnis et al discloses downscaling after decompressed video frames/pictures.

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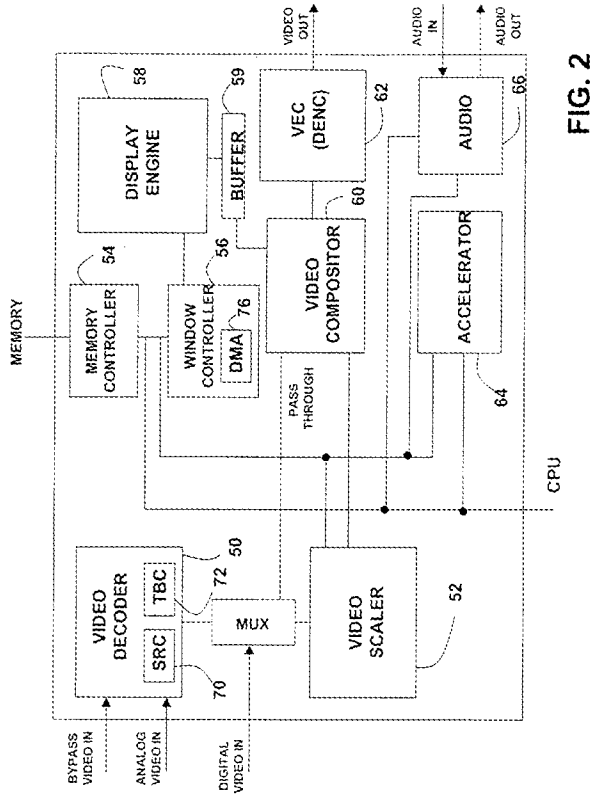


FIG. 2

Reviewing the architecture shown in Figure 2 of *MacInnis*, it is noted that analog and digital video enters at the decoder 50 and the mux, respectively. Further, column 5, 65-66 of *MacInnis* provides as follows:

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In other words, from this provision and Figure 2 of *MacInnis*, it appears that scaling is performed on the analog or video inputs. More telling of the functionality performed by the architecture in Figure 2 is the description set forth in the same paragraph in column 6, lines 4-9 of *MacInnins*, reproduced below (emphasis added):

> Any portion of the input may be the source for video scaling. To conserve memory and bandwidth, the video scaler preferably downscales before capturing video frames to memory, and upscales after reading from memory, but preferably does not perform both upscaling and downscaling at the same time.

In other words, scaling operations in *MacInnis* appear to be intended, at least in part, to reduce memory consumption. Further, these excerpts also highlight the differences to the claims of the present application, the latter being in the context of scaling operations performed on video already saved to memory. The reference in the above-reproduced section of the final Office Action to the alleged similarity to Appellants' decoder in Figure 4 ignores the fact that the decoder in Figure 4 of Appellants' disclosure acts on video stored in media memory 60 and is passed to the media engine 80 that encompasses the video decoder via the media memory bus, and further, that the scaling operation in Appellant's claimed embodiment is implemented downstream of the media memory, unlike that shown in Figure 2 of *MacInnis*.

Likewise, *Kalra*, though apparently used for alleged teaching of the various mode operations as described in claim 54, appears to scale the video in the network (by sending base and additive streams based on a profile provided by the client (see Summary, e.g., col. 2, lines 27-49, *Kalra*), addressing the presence of clients of differing capabilities in a network (see Background, e.g., col. 1, lines 21-58, *Kalra*). In other words, any reduction of resolution via scaling occurs pre-capture, not post-capture as claimed.

With regard to *Boyce*, the final Office Action (page 6) alleges the following (emphasis in original):

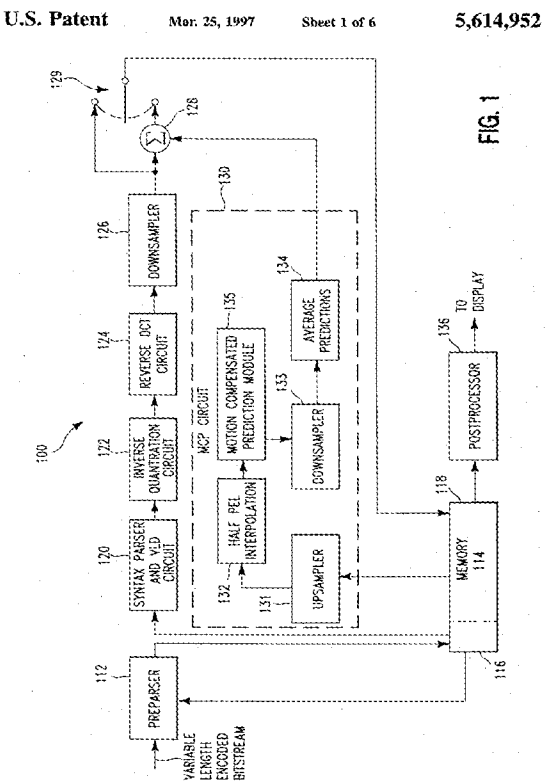
> Furthermore, Boyce et al teaches digital video decoder comprising retrieving a set of compressed pictures/frames from a first portion (Fig. 1, 116) of a memory component (114), wherein the memory component stores decoded video pictures/frames in a distinct second portion (116) of the memory component, wherein the set of video frames corresponding to video pictures/frames (col. 4, lines 64-67; col. 5, lines 1-4; col. 10, lines 44-50), and transferring a set of retrieved decoded pictures/frames (Fig. 4, 402, 403) to a display device (To Display) ***while*** scaling video pictures/frames in transit to the display device to a second spatial (reduced) resolution ***without*** storing pictures in a memory component, wherein the second spatial resolution is smaller than the first spatial resolution (from 401 or 402) for efficiently managing the memory resources such

> as size or the bandwidth (col. 10, lines 1-4) and implementing picture-in-picture capabilities in a digital TV without incurring the cost of multiple full resolution decoders (col. 17, lines 66-67; col. 18, lines 12-38; col. 2, lines 37-40).

Appellants respectfully submit that *Boyce*, like *MacInnis* and *Kalra*, fails to describe downscaling (e.g., scaling to a reduced resolution as claimed) after the decompressed picture buffer. It is noteworthy that the reduced resolution decoders 402 and 403 of FIG. 4 are used in the final Office Action to support the alleged teachings of downscaling in transit. However, Appellants believe that *Boyce* teaches that the decoders 402 and 403 are based on the operations and architecture of the decoder circuit 100 shown, for instance in Figure 1 of *Boyce*. For instance, *Boyce* describes the decoders 402 and 403 as containing components of the decoder circuit 100 (reproduced below), such as the IDCT circuit 124 (col. 18, line 16, *Boyce*), the IQ circuit 122 (col. 18, line 28, *Boyce*), and preparser 112 (col. 18, lines 39-46, *Boyce*). Further, the decoders 402 and 403 are described in col. 18, lines 33-38 of *Boyce* as follows (emphasis added):

> In accordance with the present invention, the reduced resolution decoders 402, 403 store the low resolution frames in their reduced size. Thus, by using 2.times.2 DCT coefficient blocks the size of the frame buffers can be about 1/16th of the size that would be required if 8.times.8 DCT coefficient blocks, i.e., full resolution blocks, were stored.

In other words, the decoders 402 and 403 not only store frames in reduced resolution format (and hence do NOT teach downscaling after the decompressed picture buffer), but also appear to share the same architecture as the decoder circuit 100. Figure 1 of *Boyce* is reproduced below:




The following excerpts from *Boyce* (reproduced below) support Appellants' position that *Boyce* (like *Kalra* and *MacInnis*) operates in a fundamentally different manner than claimed (emphasis added):

> *Col. 4, lines 34-39*: The method of the present invention for decoding HD and SD pictures includes the steps of reducing the resolution of received HD pictures prior to decoding by using, e.g., a preparser unit and/or adaptive field/frame downsampling to reduce the complexity of later processing stages of the decoder.
>
> *Col. 5, lines 25-44*: Because the cost and complexity of a HDTV decoder is largely a function of the requirement that it process large amounts of data on a real time basis, it is possible to reduce the complexity and thus the cost of a HDTV compatible decoder by reducing the amount of data that needs to be processed. While using only a small portion of the video data received in an HDTV signal will result in reduced resolution and picture quality, by carefully selecting which HDTV data to process and the method by which it is processed, video image quality comparable to or better than SD television signals can be achieved. As will be discussed below, the preparser 112 serves to dynamically limit the amount of video data supplied to the remaining elements of the decoder

> circuit 100 including the syntax parser and VLD circuit 120 thereby reducing the amount of data that must be processed by the subsequent circuit elements on a real time basis and the required complexity of those circuit elements. An additional benefit of the use of the preparser 112 is that it permits for the use of a smaller coded data buffer 116 than would otherwise be required.
>
> *Col. 9, line 61 – col. 10, line 5*: The output of the IDCT circuit 124 is coupled to the input of the downsampler 126. The downsampler 126 is used to downsample the data corresponding to each picture prior to storage in the frame buffer 118. As a result of the downsampling operation, the amount of data required to represent a video frame is substantially reduced. For example if the downsampler 126 is implemented to remove half of the digital samples used to represent a picture, the amount of data that would have to be stored will be reduced by a factor of approximately two substantially reducing the amount of memory required to implement the frame buffer 118.
>
> *Col. 11, lines 39-46*: In accordance with the present invention, the downsampled frames supplied by the frame buffer 118 to the MCP circuit 130 are upsampled, e.g., on-the-fly, interpolated and then downsampled prior to generating predictions based on the motion vectors. In this manner the motion vectors which were originally generated based on full resolution video frames are effectively applied to downsampled video frames.

These excerpts from *Boyce* reveal that downsampling does not occur post-capture in a decoded picture buffer, but rather, pre-capture. The final Office Action (page 2, "Response to Remarks") provides as follows:

> Moreover, Boyce et al not only teaches storing frames in reduce resolution, but also teaches downscaling by performing IDCT (inverse discrete cosine transform) and IQ (inverse quantization)(col. 18, lines 12-38). In other words, the reduced resolution decoder inherently has to downscale a standard frame into a much smaller size frame in order to display the reduced frame into the main frame itself as a picture in picture format as discussed above.

Col. 18, lines 12-38 of *Boyce* provides as follows:

> In one embodiment of the present invention the size of the reduced resolution pictures incorporated into the main picture is selected to be 1/4.times.1/4 the size of the normal picture. In such an embodiment, each MPEG 8.times.8 pixel block need only be decoded to a size corresponding to a block of 2.times.2 pixels.
>
> The cost of the IDCT circuit 124 used in the reduced resolution decoders 402, 403 can be substantially reduced in accordance with the present invention by performing the IDCT operations on only 2.times.2 blocks as opposed to 8.times.8 blocks. This is achieved by, e.g., retaining and processing only the upper left 2.times.2 block of DCT coefficients of each 8.times.8 DCT coefficient block of a HDTV picture with all the other DCT coefficients being set to zero. Accordingly, in

> such an embodiment, the IDCT circuit cost is reduced to approximately the cost of a circuit which can perform a 2.times.2 IDCT as opposed to an 8.times.8 IDCT.
>
> The IQ circuit 122 of the reduced resolution decoders 402, 403 can be simplified in a similar manner with the IQ circuit 122 operating only on a 2.times.2 block of DCT coefficients, i.e., 4 coefficient values, as opposed to 64 DCT coefficient values that form an 8.times.8 DCT coefficient block.
>
> In accordance with the present invention, the reduced resolution decoders 402, 403 store the low resolution frames in their reduced size. Thus, by using 2.times.2 DCT coefficient blocks the size of the frame buffers can be about 1/16th of the size that would be required if 8.times.8 DCT coefficient blocks, i.e., full resolution blocks, were stored.

Nothing in the section recited above suggests downscaling post capture. Indeed, the reference to IDCT and IQ components is misplaced, since those components are shown in Figure 1 of *Boyce* as receiving compressed pictures (section 116 is a "coded data buffer" that is "used for the temporary storage of the compressed bitstream" – see, col. 4, line 67 – col. 5, line 1, *Boyce*), and hence cannot constitute the retrieval of reconstructed frames as claimed. For at least these reasons, Appellants respectfully submit that claim 54 is allowable over *MacInnis* in view of *Boyce* and *Kalra* and respectfully request that the rejection be overturned.

Because independent claim 54 is allowable over *MacInnis* in view of *Boyce* and *Kalra*, dependent claims 78, 80-81, and 87 are allowable as a matter of law. Accordingly, Appellants respectfully request that the rejection to dependent claims 78, 80-81, and 87 be overturned for similar reasons expressed above for claim 54.

4. Independent claim 55 and dependent claims 82 and 88

Claim 55 recites (with emphasis added):

> 55. A method for adapting to resource constraints of a digital home communication terminal (DHCT), said method comprising steps of:
> operating the DHCT in either a non-resource constrained mode or one of a plurality of resource-constrained modes, the DHCT capable of operating in the non-resource constrained mode and the plurality of resource-constrained modes;
> receiving, in a memory component, ***video frames each comprising a complete picture***;

determining whether one of the resource-constrained modes is to be initiated;

responsive to determining that one of the resource-constrained modes is to be initiated, initiating the resource-constrained mode, including:

***retrieving the video frames from the memory component; and***

***transferring the retrieved video frames to a display device while downscaling the retrieved video frames in transit to the display device.***

Appellants respectfully submit that claim 55 is allowable over the combination of *MacInnis* in view of *Boyce* and *Kalra*. Briefly, claim 55 comprises elements that are arranged to cover at least one embodiment where video frames each corresponding to a complete (e.g., reconstructed) picture is stored in memory, and retrieval from the memory occurs whereby through transfer to a display device, downscaling is achieved in transit. In contrast, Appellants respectfully submit that the cited art of record operates in a fundamentally different manner.

For instance, with regard to *MacInnis*, the final Office Action (page 7, emphasis in original) acknowledges that *MacInnis* does not "seem to particularly disclose…transferring the set of retrieved reconstructed decompressed video data to a display device ***while*** *downscaling the video picture in transit to the display device*." Though *MacInnis* appears to focus attention on primarily graphics processing, *MacInnis* describes video decoding and capture and scaling at least in association with Figure 5 (reproduced below).

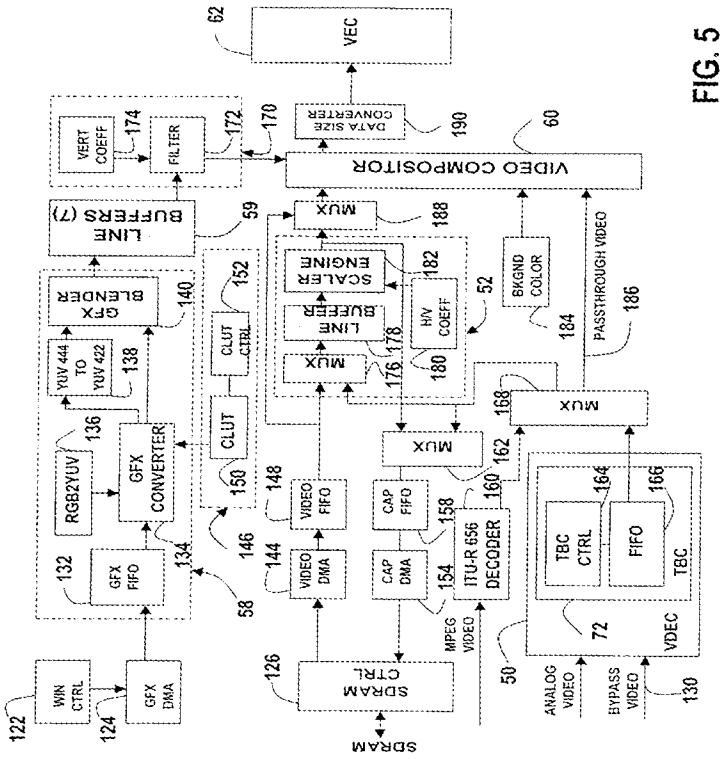



FIG. 5

In particular, col. 11, lines 39 – col. 12, line 7 of *MacInnis* provides as follows (emphasis added):

> Analog video or MPEG video may be provided to the video compositor as passthrough video. Alternatively, either type of video may be captured into memory and provided to the video compositor as a scaled video window. The digitized analog video signals preferably have a pixel sample rate of 13.5 MHz, contain a 16 bit data stream in YUV 4:2:2 format, and include timing signals such as top field and vertical sync signals.
>
> The VDEC 50 includes a time base corrector (TBC) 72 comprising a TBC controller 164 and a FIFO 166. To provide passthrough video that is synchronized to a display clock preferably without using a frame buffer, the digitized analog video is corrected in the time domain in the TBC 72 before being blended with other graphics and video sources. During time base correction, the video input which runs nominally at 13.5 MHZ is synchronized with the display clock which runs nominally at 13.5 MHZ at the output; these two frequencies that

> are both nominally 13.5 MHz are not necessarily exactly the same frequency. In the TBC, the video output is preferably offset from the video input by a half scan line per field.
>
> A capture FIFO 158 and a capture DMA 154 preferably capture the digitized analog video signals and MPEG video. The SDRAM controller 126 provides captured video frames to the external SDRAM. A video DMA 144 transfers the captured video frames to a video FIFO 148 from the external SDRAM.
>
> The digitized analog video signals and MPEG video are preferably scaled down to less than 100% prior to being captured and are scaled up to more than 100% after being captured. The video scaler 52 is shared by both upscale and downscale operations. The video scaler preferably includes a multiplexer 176, a set of line buffers 178, a horizontal and vertical coefficient memory 180 and a scaler engine 182. The scaler engine 182 preferably includes a set of two polyphase filters, one for each of horizontal and vertical dimensions.

In other words, it is clear that any alleged "downscaling" occurs prior to capture, not post-capture as described in association with claim 55. Such operation is consistent with *MacInnis*' expressed benefit (see Summary) of conserving memory.

The final Office Action (page 2, "Response to Remarks," emphasis in original) provides as follows:

> Moreover, please note Macinnis et al discloses video decoder (Fig. 2, 50) to the video scaler (Fig. 2, 52), wherein the scaler may perform both downscaling and upscaling of digital/analog video as needed (col. 5, lines 65-66), which is substantially the same/similar as Applicant's decoder (Fig. 4, 81) to the video scaler (83). Therefore, Macinnis et al discloses downscaling after decompressed video frames/pictures.

Appellants respectfully disagree. FIG. 2 of *MacInnis* provides as follows:

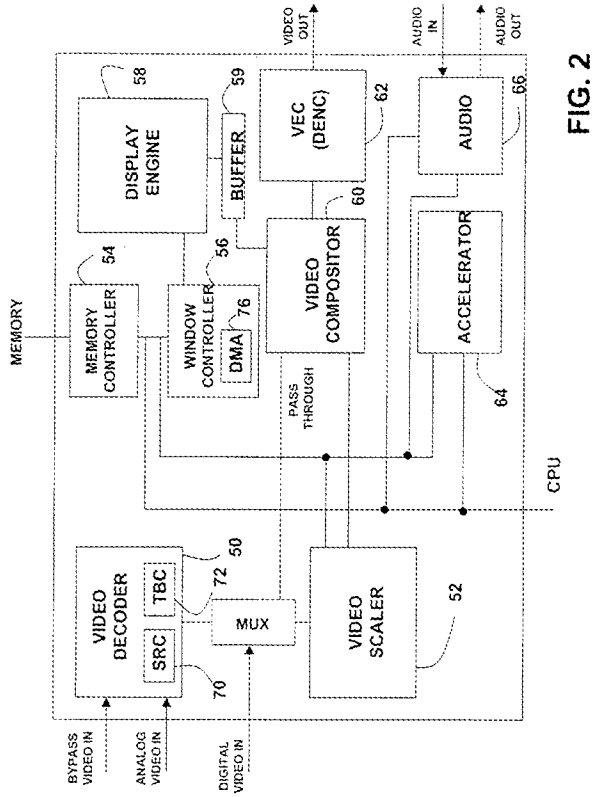



FIG. 2

Reviewing the architecture shown in Figure 2 of *MacInnis*, it is noted that analog and digital video enters at the decoder 50 and the mux, respectively. Further, column 5, 65-66 of *MacInnis* provides as follows:

> The video scaler 52 may perform both downscaling and upscaling of digital video and analog video as needed.

In other words, from this provision and Figure 2 of *MacInnis*, it appears that scaling is performed on the analog or video inputs. More telling of the functionality performed by the architecture in Figure 2 is the description set forth in the same paragraph in column 6, lines 4-9 of *MacInnins*, reproduced below (emphasis added):

> Any portion of the input may be the source for video scaling. To conserve memory and bandwidth, the video scaler preferably downscales before capturing video frames to memory, and upscales after reading from memory, but preferably does not perform both upscaling and downscaling at the same time.

In other words, scaling operations in *MacInnis* appear to be intended, at least in part, to reduce memory consumption. Further, these excerpts also highlight the differences to the claims of the present application, the latter being in the context of scaling operations performed on video already saved to memory. The reference in the above-reproduced section of the final Office Action to the alleged similarity to Appellants' decoder in Figure 4 ignores the fact that the decoder in Figure 4 of Appellants' disclosure acts on video stored in media memory 60 and is passed to the media engine 80 that encompasses the video decoder via the media memory bus, and further, that the scaling operation in Appellant's claimed embodiment is implemented downstream of the media memory, unlike that shown in Figure 2 of *MacInnis*.

Likewise, *Kalra*, though apparently used for alleged teaching of the various mode operations as described in claim 55, appears to scale the video in the network (by sending base and additive streams based on a profile provided by the client (see Summary, e.g., col. 2, lines 27-49, *Kalra*), addressing the presence of clients of differing capabilities in a network (see Background, e.g., col. 1, lines 21-58, *Kalra*). In other words, any reduction of resolution via scaling occurs pre-capture, not post-capture as claimed.

With regard to *Boyce*, the final Office Action (page 8) alleges the following (emphasis in original):

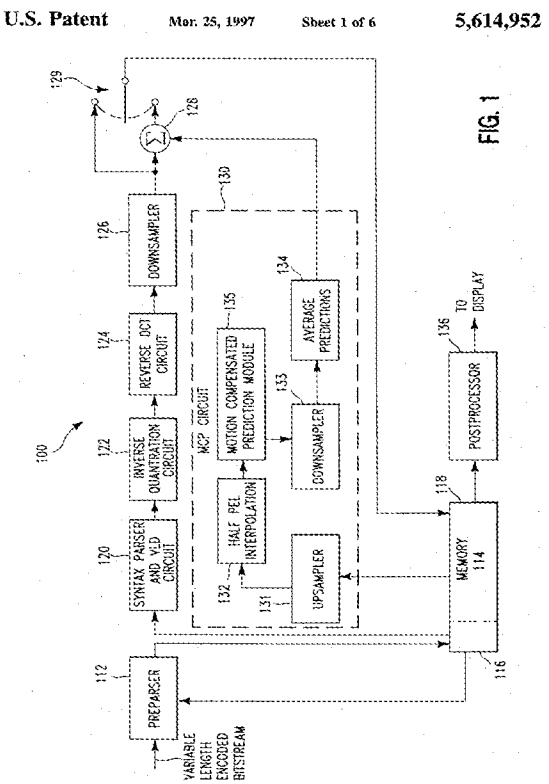
> Furthermore, Boyce et al teaches transferring the set of retrieved reconstructed decompressed (decoded) video frames (Fig. 4, 402, 403) to a display device (TO DISPLAY) ***while*** downscaling (Reduced Resolution) the video picture in transit to the display device for implementing picture-in-picture capabilities in a digital TV without incurring the cost of multiple full resolution decoders (Fig. 4, col. 17, lines 66-67; col. 18, lines 1-16; col. 2, lines 37-40).

Appellants respectfully submit that *Boyce*, like *MacInnis* and *Kalra*, fails to describe downscaling (e.g., scaling to a reduced resolution as claimed) after the decompressed picture buffer. It is

noteworthy that the reduced resolution decoders 402 and 403 of FIG. 4 are used in the final Office Action to support the alleged teachings of downscaling in transit. However, Appellants believe that *Boyce* teaches that the decoders 402 and 403 are based on the operations and architecture of the decoder circuit 100 shown, for instance in Figure 1 of *Boyce*. For instance, *Boyce* describes the decoders 402 and 403 as containing components of the decoder circuit 100 (reproduced below), such as the IDCT circuit 124 (col. 18, line 16, *Boyce*), the IQ circuit 122 (col. 18, line 28, *Boyce*), and preparser 112 (col. 18, lines 39-46, *Boyce*). Further, the decoders 402 and 403 are described in col. 18, lines 33-38 of *Boyce* as follows (emphasis added):

> In accordance with the present invention, the reduced resolution decoders 402, 403 store the low resolution frames in their reduced size. Thus, by using 2.times.2 DCT coefficient blocks the size of the frame buffers can be about 1/16th of the size that would be required if 8.times.8 DCT coefficient blocks, i.e., full resolution blocks, were stored.

In other words, the decoders 402 and 403 not only store frames in reduced resolution format (and hence do NOT teach downscaling after the decompressed picture buffer), but also appear to share the same architecture as the decoder circuit 100. Figure 1 of *Boyce* is reproduced below:




The following excerpts from *Boyce* (reproduced below) support Appellants' position that *Boyce* (like *Kalra* and *MacInnis*) operates in a fundamentally different manner than claimed (emphasis added):

> *Col. 4, lines 34-39*: The method of the present invention for decoding HD and SD pictures includes the steps of reducing the resolution of received HD pictures prior to decoding by using, e.g., a preparser unit and/or adaptive field/frame downsampling to reduce the complexity of later processing stages of the decoder.
>
> *Col. 5, lines 25-44*: Because the cost and complexity of a HDTV decoder is largely a function of the requirement that it process large amounts of data on a real time basis, it is possible to reduce the complexity and thus the cost of a HDTV compatible decoder by reducing the amount of data that needs to be processed. While using only a small portion of the video data received in an HDTV signal will result in reduced resolution and picture quality, by carefully selecting which HDTV data to process and the method by which it is processed, video image quality comparable to or better than SD television signals can be achieved. As will be discussed below, the preparser 112 serves to dynamically limit the amount of video data supplied to the remaining elements of the decoder

> circuit 100 including the syntax parser and VLD circuit 120 thereby reducing the amount of data that must be processed by the subsequent circuit elements on a real time basis and the required complexity of those circuit elements. An additional benefit of the use of the preparser 112 is that it permits for the use of a smaller coded data buffer 116 than would otherwise be required.
>
> *Col. 9, line 61 – col. 10, line 5*: The output of the IDCT circuit 124 is coupled to the input of the downsampler 126. The downsampler 126 is used to downsample the data corresponding to each picture prior to storage in the frame buffer 118. As a result of the downsampling operation, the amount of data required to represent a video frame is substantially reduced. For example if the downsampler 126 is implemented to remove half of the digital samples used to represent a picture, the amount of data that would have to be stored will be reduced by a factor of approximately two substantially reducing the amount of memory required to implement the frame buffer 118.
>
> *Col. 11, lines 39-46*: In accordance with the present invention, the downsampled frames supplied by the frame buffer 118 to the MCP circuit 130 are upsampled, e.g., on-the-fly, interpolated and then downsampled prior to generating predictions based on the motion vectors. In this manner the motion vectors which were originally generated based on full resolution video frames are effectively applied to downsampled video frames.

These excerpts from *Boyce* reveal that downsampling does not occur post-capture in a decoded picture buffer, but rather, pre-capture. The final Office Action (page 2, "Response to Remarks") provides as follows:

> Moreover, Boyce et al not only teaches storing frames in reduce resolution, but also teaches downscaling by performing IDCT (inverse discrete cosine transform) and IQ (inverse quantization)(col. 18, lines 12-38). In other words, the reduced resolution decoder inherently has to downscale a standard frame into a much smaller size frame in order to display the reduced frame into the main frame itself as a picture in picture format as discussed above.

Col. 18, lines 12-38 of *Boyce* provides as follows:

> In one embodiment of the present invention the size of the reduced resolution pictures incorporated into the main picture is selected to be 1/4.times.1/4 the size of the normal picture. In such an embodiment, each MPEG 8.times.8 pixel block need only be decoded to a size corresponding to a block of 2.times.2 pixels.
>
> The cost of the IDCT circuit 124 used in the reduced resolution decoders 402, 403 can be substantially reduced in accordance with the present invention by performing the IDCT operations on only 2.times.2 blocks as opposed to 8.times.8 blocks. This is achieved by, e.g., retaining and processing only the upper left 2.times.2 block of DCT coefficients of each 8.times.8 DCT coefficient block of a HDTV picture with all the other DCT coefficients being set to zero. Accordingly, in

> such an embodiment, the IDCT circuit cost is reduced to approximately the cost of a circuit which can perform a 2.times.2 IDCT as opposed to an 8.times.8 IDCT.
>
> The IQ circuit 122 of the reduced resolution decoders 402, 403 can be simplified in a similar manner with the IQ circuit 122 operating only on a 2.times.2 block of DCT coefficients, i.e., 4 coefficient values, as opposed to 64 DCT coefficient values that form an 8.times.8 DCT coefficient block.
>
> In accordance with the present invention, the reduced resolution decoders 402, 403 store the low resolution frames in their reduced size. Thus, by using 2.times.2 DCT coefficient blocks the size of the frame buffers can be about 1/16th of the size that would be required if 8.times.8 DCT coefficient blocks, i.e., full resolution blocks, were stored.

Nothing in the section recited above suggests downscaling post capture. Indeed, the reference to IDCT and IQ components is misplaced, since those components are shown in Figure 1 of *Boyce* as receiving compressed pictures (section 116 is a "coded data buffer" that is "used for the temporary storage of the compressed bitstream" – see, col. 4, line 67 – col. 5, line 1, *Boyce*), and hence cannot constitute the retrieval of reconstructed frames as claimed. For at least these reasons, Appellants respectfully submit that claim 55 is allowable over *MacInnis* in view of *Boyce* and *Kalra* and respectfully request that the rejection be overturned.

Because independent claim 55 is allowable over *MacInnis* in view of *Boyce* and *Kalra*, dependent claims 82 and 88 are allowable as a matter of law. Accordingly, Appellants respectfully request that the rejection to dependent claims 82 and 88 be overturned for similar reasons expressed above for claim 55.

5. Independent claim 89

Claim 89 recites (with emphasis added):

> 89. A method, comprising:
> retrieving, from a first portion of a memory component, a set of compressed frames;
> storing, in a second and distinct portion of the memory component, a set of decoded frames corresponding to the set of compressed frames, each of the set of ***decoded frames being at a first spatial resolution***;

***retrieving, from the second and distinct portion of the memory component, the set of decoded frames; and***

***transferring the retrieved set of decoded frames to a display device while scaling the frames in transit to the display device to a second spatial resolution without storing the frames in the memory component, wherein the second spatial resolution is smaller than the first spatial resolution***.

Appellants respectfully submit that claim 89 is allowable over the combination of *MacInnis* in view of *Boyce* and *Kalra*. Briefly, claim 89 comprises elements that are arranged to cover at least one embodiment where a compressed picture buffer and decoded picture buffer reside in media memory, and downscaling is implemented on the video picture in transit between the decoded picture buffer and the display device. In contrast, Appellants respectfully submit that the cited art of record operates in a fundamentally different manner.

For instance, with regard to *MacInnis*, the final Office Action (page 6) acknowledges that *MacInnis* does not "seem to particularly disclose the memory component storing and retrieving a set of decoded pictures in a distinct second portion," and further acknowledges (page 6, emphasis in original) that *MacInnis* "does not seem to particularly disclose…transferring a set of retrieved decoded pictures to a display device ***while*** *scaling the video picture in transit to the display device to a second spatial resolution* ***without*** *storing pictures in a memory component,* wherein the second spatial resolution is smaller than the first spatial resolution." Though *MacInnis* appears to focus attention on primarily graphics processing, *MacInnis* describes video decoding and capture and scaling at least in association with Figure 5 (reproduced below).

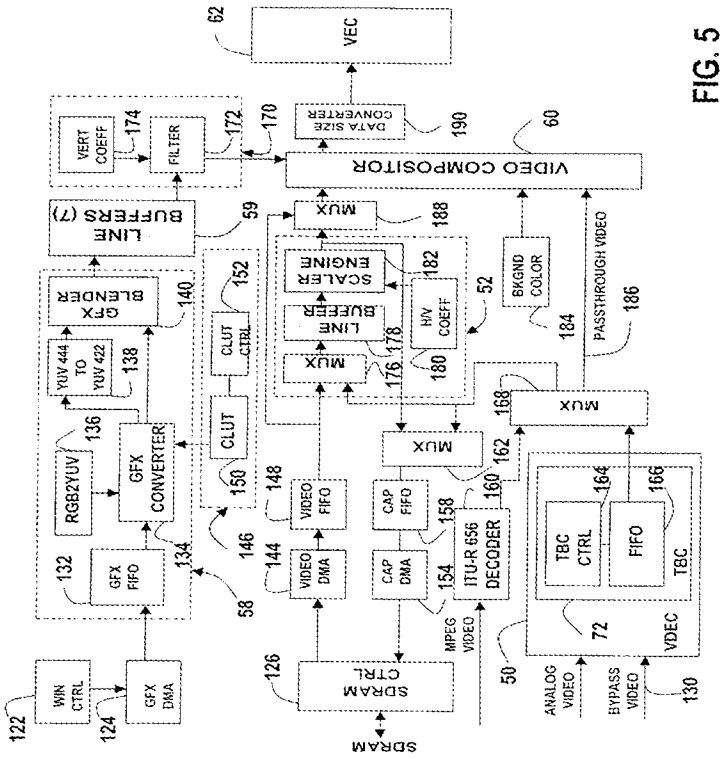



FIG. 5

In particular, col. 11, lines 39 – col. 12, line 7 of *MacInnis* provides as follows (emphasis added):

> Analog video or MPEG video may be provided to the video compositor as passthrough video. Alternatively, either type of video may be captured into memory and provided to the video compositor as a scaled video window. The digitized analog video signals preferably have a pixel sample rate of 13.5 MHz, contain a 16 bit data stream in YUV 4:2:2 format, and include timing signals such as top field and vertical sync signals.
>
> The VDEC 50 includes a time base corrector (TBC) 72 comprising a TBC controller 164 and a FIFO 166. To provide passthrough video that is synchronized to a display clock preferably without using a frame buffer, the digitized analog video is corrected in the time domain in the TBC 72 before being blended with other graphics and video sources. During time base correction, the video input which runs nominally at 13.5 MHZ is synchronized with the display clock which runs nominally at 13.5 MHZ at the output; these two frequencies that

> are both nominally 13.5 MHz are not necessarily exactly the same frequency. In the TBC, the video output is preferably offset from the video input by a half scan line per field.
>
> A capture FIFO 158 and a capture DMA 154 preferably capture the digitized analog video signals and MPEG video. The SDRAM controller 126 provides captured video frames to the external SDRAM. A video DMA 144 transfers the captured video frames to a video FIFO 148 from the external SDRAM.
>
> The digitized analog video signals and MPEG video are preferably scaled down to less than 100% prior to being captured and are scaled up to more than 100% after being captured. The video scaler 52 is shared by both upscale and downscale operations. The video scaler preferably includes a multiplexer 176, a set of line buffers 178, a horizontal and vertical coefficient memory 180 and a scaler engine 182. The scaler engine 182 preferably includes a set of two polyphase filters, one for each of horizontal and vertical dimensions.

In other words, it is clear that any alleged "downscaling" (i.e., in claim 89, scaling that results in a smaller resolution than the first resolution from which it derives) occurs prior to capture, not post-capture as described in association with claim 89. Such operation is consistent with *MacInnis*' expressed benefit (see Summary) of conserving memory.

The final Office Action (page 2, "Response to Remarks," emphasis in original) provides as follows:

> Moreover, please note Macinnis et al discloses video decoder (Fig. 2, 50) to the video scaler (Fig. 2, 52), wherein the scaler may perform both downscaling and upscaling of digital/analog video as needed (col. 5, lines 65-66), which is substantially the same/similar as Applicant's decoder (Fig. 4, 81) to the video scaler (83). Therefore, Macinnis et al discloses downscaling after decompressed video frames/pictures.

Appellants respectfully disagree. FIG. 2 of *MacInnis* provides as follows:

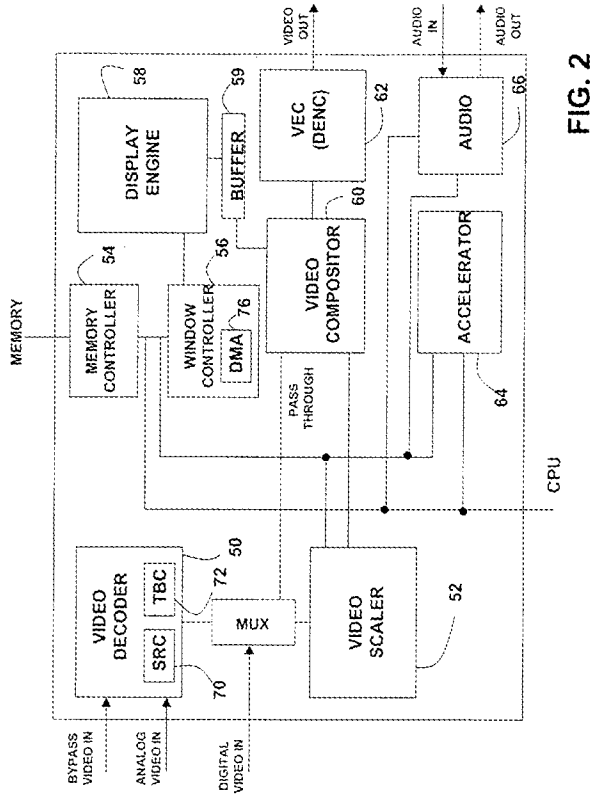



FIG. 2

Reviewing the architecture shown in Figure 2 of *MacInnis*, it is noted that analog and digital video enters at the decoder 50 and the mux, respectively. Further, column 5, 65-66 of *MacInnis* provides as follows:

> The video scaler 52 may perform both downscaling and upscaling of digital video and analog video as needed.

In other words, from this provision and Figure 2 of *MacInnis*, it appears that scaling is performed on the analog or video inputs. More telling of the functionality performed by the architecture in Figure 2 is the description set forth in the same paragraph in column 6, lines 4-9 of *MacInnins*, reproduced below (emphasis added):

> Any portion of the input may be the source for video scaling. To conserve memory and bandwidth, the video scaler preferably downscales before capturing video frames to memory, and upscales after reading from memory, but preferably does not perform both upscaling and downscaling at the same time.

In other words, scaling operations in *MacInnis* appear to be intended, at least in part, to reduce memory consumption. Further, these excerpts also highlight the differences to the claims of the present application, the latter being in the context of scaling operations performed on video already saved to memory. The reference in the above-reproduced section of the final Office Action to the alleged similarity to Appellants' decoder in Figure 4 ignores the fact that the decoder in Figure 4 of Appellants' disclosure acts on video stored in media memory 60 and is passed to the media engine 80 that encompasses the video decoder via the media memory bus, and further, that the scaling operation in Appellant's claimed embodiment is implemented downstream of the media memory, unlike that shown in Figure 2 of *MacInnis*.

Likewise, *Kalra*, though apparently used for alleged teaching of the various mode operations as described in claim 89, appears to scale the video in the network (by sending base and additive streams based on a profile provided by the client (see Summary, e.g., col. 2, lines 27-49, *Kalra*), addressing the presence of clients of differing capabilities in a network (see Background, e.g., col. 1, lines 21-58, *Kalra*). In other words, any reduction of resolution via scaling occurs pre-capture, not post-capture as claimed.

With regard to *Boyce*, the final Office Action (page 6) alleges the following (emphasis in original):

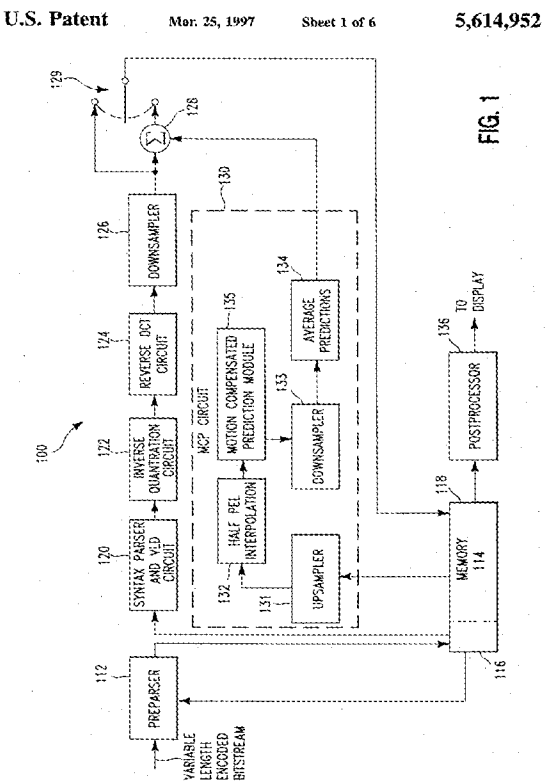
> Furthermore, Boyce et al teaches digital video decoder comprising retrieving a set of compressed pictures/frames from a first portion (Fig. 1, 116) of a memory component (114), wherein the memory component stores decoded video pictures/frames in a distinct second portion (116) of the memory component, wherein the set of video frames corresponding to video pictures/frames (col. 4, lines 64-67; col. 5, lines 1-4; col. 10, lines 44-50), and transferring a set of retrieved decoded pictures/frames (Fig. 4, 402, 403) to a display device (To Display) ***while*** scaling video pictures/frames in transit to the display device to a second spatial (reduced) resolution ***without*** storing pictures in a memory component, wherein the second spatial resolution is smaller than the first spatial resolution (from 401 or 402) for efficiently managing the memory resources such

> as size or the bandwidth (col. 10, lines 1-4) and implementing picture-in-picture capabilities in a digital TV without incurring the cost of multiple full resolution decoders (col. 17, lines 66-67; col. 18, lines 12-38; col. 2, lines 37-40).

Appellants respectfully submit that *Boyce*, like *MacInnis* and *Kalra*, fails to describe downscaling (e.g., scaling to a reduced resolution as claimed) after the decompressed picture buffer. It is noteworthy that the reduced resolution decoders 402 and 403 of FIG. 4 are used in the final Office Action to support the alleged teachings of downscaling in transit. However, Appellants believe that *Boyce* teaches that the decoders 402 and 403 are based on the operations and architecture of the decoder circuit 100 shown, for instance in Figure 1 of *Boyce*. For instance, *Boyce* describes the decoders 402 and 403 as containing components of the decoder circuit 100 (reproduced below), such as the IDCT circuit 124 (col. 18, line 16, *Boyce*), the IQ circuit 122 (col. 18, line 28, *Boyce*), and preparser 112 (col. 18, lines 39-46, *Boyce*). Further, the decoders 402 and 403 are described in col. 18, lines 33-38 of *Boyce* as follows (emphasis added):

> In accordance with the present invention, the reduced resolution decoders 402, 403 store the low resolution frames in their reduced size. Thus, by using 2.times.2 DCT coefficient blocks the size of the frame buffers can be about 1/16th of the size that would be required if 8.times.8 DCT coefficient blocks, i.e., full resolution blocks, were stored.

In other words, the decoders 402 and 403 not only store frames in reduced resolution format (and hence do NOT teach downscaling after the decompressed picture buffer), but also appear to share the same architecture as the decoder circuit 100. Figure 1 of *Boyce* is reproduced below:




The following excerpts from *Boyce* (reproduced below) support Appellants' position that *Boyce* (like *Kalra* and *MacInnis*) operates in a fundamentally different manner than claimed (emphasis added):

> *Col. 4, lines 34-39*: The method of the present invention for decoding HD and SD pictures includes the steps of reducing the resolution of received HD pictures prior to decoding by using, e.g., a preparser unit and/or adaptive field/frame downsampling to reduce the complexity of later processing stages of the decoder.
>
> *Col. 5, lines 25-44*: Because the cost and complexity of a HDTV decoder is largely a function of the requirement that it process large amounts of data on a real time basis, it is possible to reduce the complexity and thus the cost of a HDTV compatible decoder by reducing the amount of data that needs to be processed. While using only a small portion of the video data received in an HDTV signal will result in reduced resolution and picture quality, by carefully selecting which HDTV data to process and the method by which it is processed, video image quality comparable to or better than SD television signals can be achieved. As will be discussed below, the preparser 112 serves to dynamically limit the amount of video data supplied to the remaining elements of the decoder

> circuit 100 including the syntax parser and VLD circuit 120 thereby reducing the amount of data that must be processed by the subsequent circuit elements on a real time basis and the required complexity of those circuit elements. An additional benefit of the use of the preparser 112 is that it permits for the use of a smaller coded data buffer 116 than would otherwise be required.
>
> *Col. 9, line 61 – col. 10, line 5*: The output of the IDCT circuit 124 is coupled to the input of the downsampler 126. The downsampler 126 is used to downsample the data corresponding to each picture prior to storage in the frame buffer 118. As a result of the downsampling operation, the amount of data required to represent a video frame is substantially reduced. For example if the downsampler 126 is implemented to remove half of the digital samples used to represent a picture, the amount of data that would have to be stored will be reduced by a factor of approximately two substantially reducing the amount of memory required to implement the frame buffer 118.
>
> *Col. 11, lines 39-46*: In accordance with the present invention, the downsampled frames supplied by the frame buffer 118 to the MCP circuit 130 are upsampled, e.g., on-the-fly, interpolated and then downsampled prior to generating predictions based on the motion vectors. In this manner the motion vectors which were originally generated based on full resolution video frames are effectively applied to downsampled video frames.

These excerpts from *Boyce* reveal that downsampling does not occur post-capture in a decoded picture buffer, but rather, pre-capture. The final Office Action (page 2, "Response to Remarks") provides as follows:

> Moreover, Boyce et al not only teaches storing frames in reduce resolution, but also teaches downscaling by performing IDCT (inverse discrete cosine transform) and IQ (inverse quantization)(col. 18, lines 12-38). In other words, the reduced resolution decoder inherently has to downscale a standard frame into a much smaller size frame in order to display the reduced frame into the main frame itself as a picture in picture format as discussed above.

Col. 18, lines 12-38 of *Boyce* provides as follows:

> In one embodiment of the present invention the size of the reduced resolution pictures incorporated into the main picture is selected to be 1/4.times.1/4 the size of the normal picture. In such an embodiment, each MPEG 8.times.8 pixel block need only be decoded to a size corresponding to a block of 2.times.2 pixels.
>
> The cost of the IDCT circuit 124 used in the reduced resolution decoders 402, 403 can be substantially reduced in accordance with the present invention by performing the IDCT operations on only 2.times.2 blocks as opposed to 8.times.8 blocks. This is achieved by, e.g., retaining and processing only the upper left 2.times.2 block of DCT coefficients of each 8.times.8 DCT coefficient block of a HDTV picture with all the other DCT coefficients being set to zero. Accordingly, in

> such an embodiment, the IDCT circuit cost is reduced to approximately the cost of a circuit which can perform a 2.times.2 IDCT as opposed to an 8.times.8 IDCT.
>
> The IQ circuit 122 of the reduced resolution decoders 402, 403 can be simplified in a similar manner with the IQ circuit 122 operating only on a 2.times.2 block of DCT coefficients, i.e., 4 coefficient values, as opposed to 64 DCT coefficient values that form an 8.times.8 DCT coefficient block.
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> In accordance with the present invention, the reduced resolution decoders 402, 403 store the low resolution frames in their reduced size. Thus, by using 2.times.2 DCT coefficient blocks the size of the frame buffers can be about 1/16th of the size that would be required if 8.times.8 DCT coefficient blocks, i.e., full resolution blocks, were stored.

Nothing in the section recited above suggests downscaling post capture. Indeed, the reference to IDCT and IQ components is misplaced, since those components are shown in Figure 1 of *Boyce* as receiving compressed pictures (section 116 is a “coded data buffer” that is “used for the temporary storage of the compressed bitstream” – see, col. 4, line 67 – col. 5, line 1, *Boyce*), and hence cannot constitute the retrieval of reconstructed frames as claimed. For at least these reasons, Appellants respectfully submit that claim 89 is allowable over *MacInnis* in view of *Boyce* and *Kalra* and respectfully request that the rejection be overturned.

## Conclusion

For at least the reasons discussed above, Appellants respectfully request that the Examiner's FINAL rejection of claims 38, 53-55, 71-78, 80-82, and 85-89 be overturned by the Board, and that the application be allowed to issue as a patent with pending claims 38, 53-55, 71-78, 80-82, and 85-89.

In addition to the claims listed in Section VIII (CLAIMS – APPENDIX), Section IX (EVIDENCE – APPENDIX) included herein indicates that there is no additional evidence relied upon by this brief. Section X (RELATED PROCEEDINGS – APPENDIX) included herein indicates that there are no related proceedings.

Respectfully submitted,

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## VIII. CLAIMS – APPENDIX

38. A method for adapting to resource constraints of a digital home communication terminal (DHCT), said method comprising steps of:

determining by the DHCT whether one of a resource-constrained mode or a non-resource constrained mode is to be initiated, the DHCT capable of operating in the non-resource constrained mode and a plurality of resource constrained modes;

responsive to determining that one of the resource-constrained modes is to be initiated, operating the DHCT in the determined resource-constrained mode, including:

retrieving a set of reconstructed decompressed video frames from a first portion of a memory component, wherein the memory component stores compressed video frames in a distinct second portion, wherein the set of video frames corresponds to a video picture stored in the first portion; and

transferring the set of retrieved reconstructed decompressed video frames to a display device while downscaling the video picture in transit to the display device.

53. A method for adapting to resource constraints of a digital communication terminal (DHCT), said method comprising steps of:

determining by the DHCT whether one of a plurality of resource-constrained modes is to be initiated, the DHCT capable of operating in a non-resource constrained mode and the plurality of resource-constrained modes;

responsive to determining that one of the resource-constrained modes is to be initiated, initiating the resource-constrained mode, including:

retrieving, from a first portion of a memory component, a set of compressed frames;

storing, in a second and distinct portion of the memory component, a set of decoded frames corresponding to the set of compressed frames, each of the set of decoded frames being at a first spatial resolution;

retrieving, from the second and distinct portion of the memory component, the set of decoded frames; and

transferring the retrieved set of decoded frames to a display device while scaling the frames in transit to the display device to a second spatial resolution without storing the frames in the memory component, wherein the second spatial resolution is smaller than the first spatial resolution.

54. A digital home communication terminal (DHCT) comprising:

a processor;

a circuit configured to operate in a non-resource constrained mode and a plurality of resource-constrained modes, the circuit, responsive to instantiation of operation in the resource-constrained mode, configured in cooperation with the processor to:

retrieve, from a first portion of a memory component, a set of compressed frames;

store, in a second and distinct portion of the memory component, a set of decoded frames corresponding to the set of compressed frames, each of the set of decoded frames being at a first spatial resolution;

retrieve, from the memory component, the set of decoded frames; and

transfer the set of decoded frames to a display device while scaling the frames in transit to the display device to a second spatial resolution without storing the frames in the memory component, wherein the second spatial resolution is smaller than the first spatial resolution.

55. A method for adapting to resource constraints of a digital home communication terminal (DHCT), said method comprising steps of:

operating the DHCT in either a non-resource constrained mode or one of a plurality of resource-constrained modes, the DHCT capable of operating in the non-resource constrained mode and the plurality of resource-constrained modes;

receiving, in a memory component, video frames each comprising a complete picture;

determining whether one of the resource-constrained modes is to be initiated;

responsive to determining that one of the resource-constrained modes is to be initiated, initiating the resource-constrained mode, including:

retrieving the video frames from the memory component; and

transferring the retrieved video frames to a display device while downscaling the retrieved video frames in transit to the display device.

71. The method of claim 38, further comprising:

transmitting graphics data to the display device, wherein the graphics data is displayed contemporaneously with the downscaled picture.

72. The method of claim 38, wherein the downscaling comprises horizontal scaling.

73. The method of claim 38, wherein the downscaling comprises vertical scaling.

74. The method of claim 53, further comprising the step of:

transmitting graphics data to the display device, wherein the graphics data is displayed contemporaneously with the scaled video frames.

75. The method of claim 53, wherein the scaling comprises downscaling.

76. The method of claim 53, wherein the scaling comprises horizontal scaling.

77. The method of claim 53, wherein the scaling comprises vertical scaling.

78. The DHCT of claim 54, wherein the circuit in cooperation with the processor is further configured to:

transmit graphics data to the display device, wherein the graphics data is displayed contemporaneously with the scaled frames.

80. The DHCT of claim 54, wherein the scaling comprises horizontal downscaling.

81. The DHCT of claim 54, wherein the scaling comprises vertical downscaling.

82. The method of claim 55, further comprising the step of:

transmitting graphics data to the display device, wherein the graphics data is displayed contemporaneously with the scaled video frames.

85. The method of claim 38, wherein the plurality of resource-constrained modes include a memory-constrained mode, a bus bandwidth constrained mode, and a memory and bus-bandwidth constrained mode.

86. The method of claim 53, wherein the plurality of resource-constrained modes include a memory-constrained mode, a bus bandwidth constrained mode, and a memory and bus-bandwidth constrained mode.

87. The DHCT of claim 54, wherein the plurality of resource-constrained modes include a memory-constrained mode, a bus bandwidth constrained mode, and a memory and bus-bandwidth constrained mode.

88. The method of claim 55, wherein the plurality of resource-constrained modes include a memory-constrained mode, a bus bandwidth constrained mode, and a memory and bus-bandwidth constrained mode.

89. A method, comprising:

retrieving, from a first portion of a memory component, a set of compressed frames;

storing, in a second and distinct portion of the memory component, a set of decoded frames corresponding to the set of compressed frames, each of the set of decoded frames being at a first spatial resolution;

retrieving, from the second and distinct portion of the memory component, the set of decoded frames; and

transferring the retrieved set of decoded frames to a display device while scaling the frames in transit to the display device to a second spatial resolution without storing the frames in the memory component, wherein the second spatial resolution is smaller than the first spatial resolution.

## IX. EVIDENCE – APPENDIX

None.

## X. RELATED PROCEEDINGS – APPENDIX

None.